

# SLINKY Pavilion 14''

## Intel Tiger Lake-U

### UMA

203032-1

<Core Design>

緯創資通

**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A4

Document Number

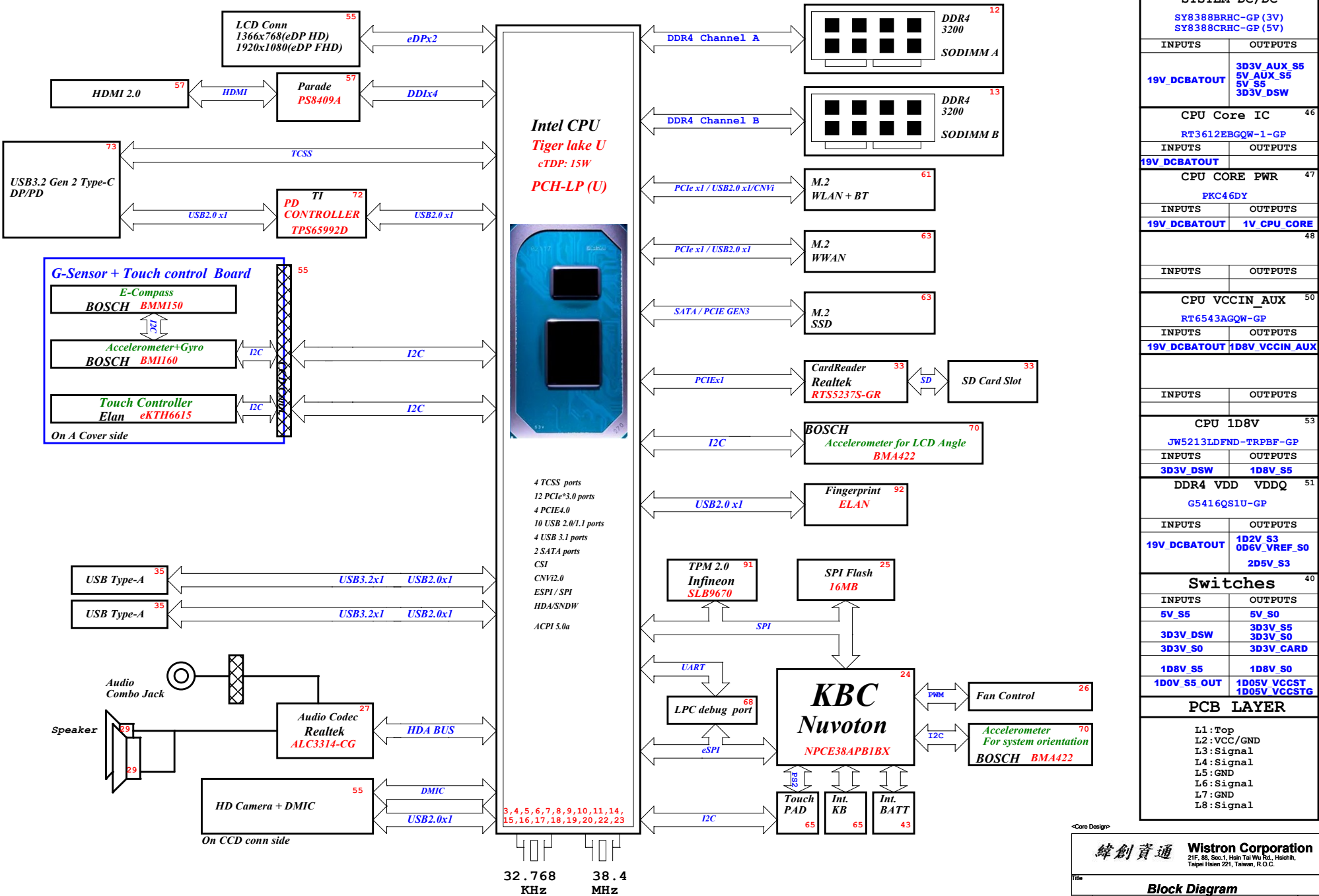
**Slinky TGL 14" Pavlion**

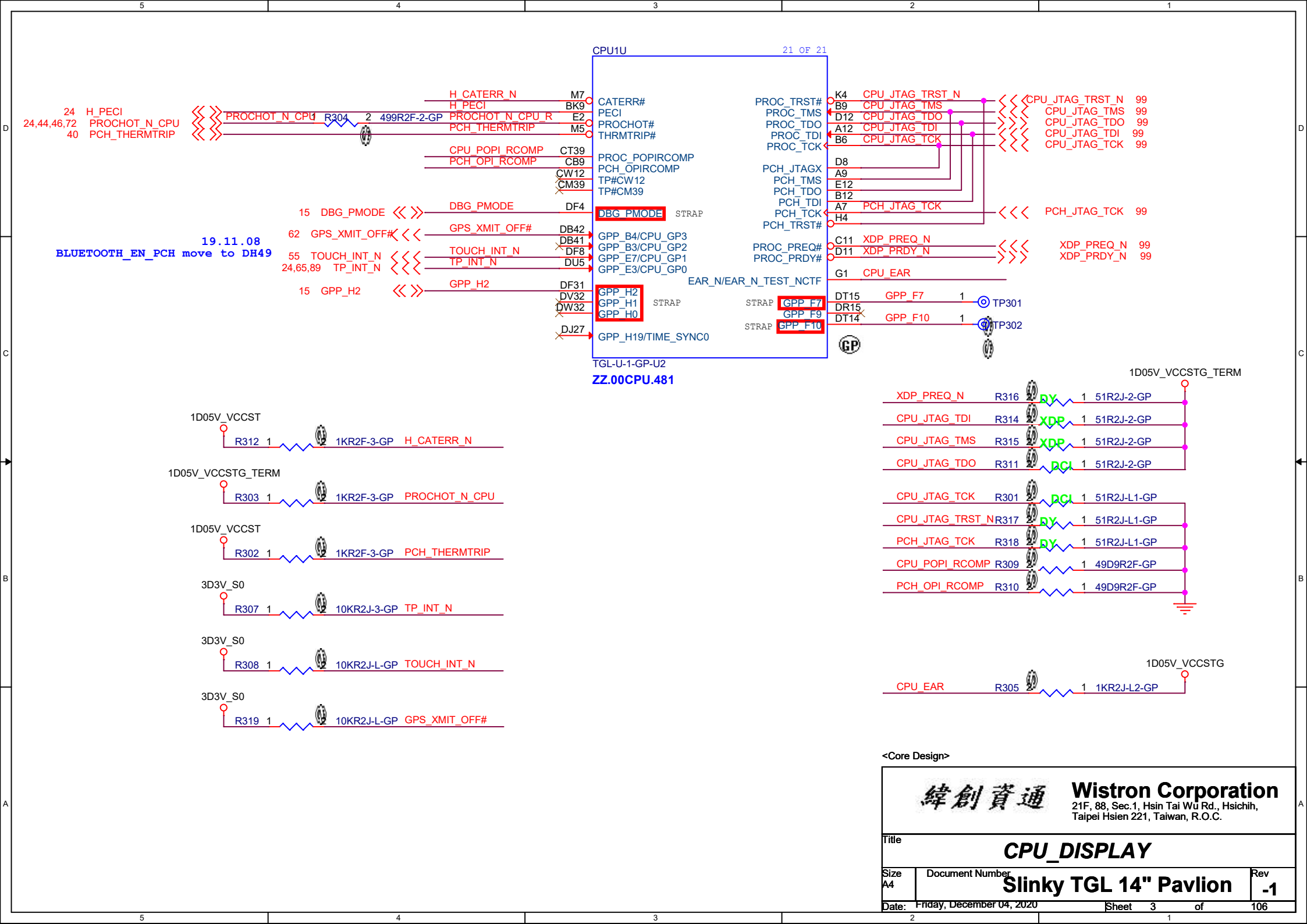
Rev  
**-1**

Date: Friday, December 04, 2020

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SLINKY Pavilion 14" Block Diagram





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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU\_DISPLAY

Size

A4

Document Number

Slinky TGL 14" Pavlion

Rev

-1

Date

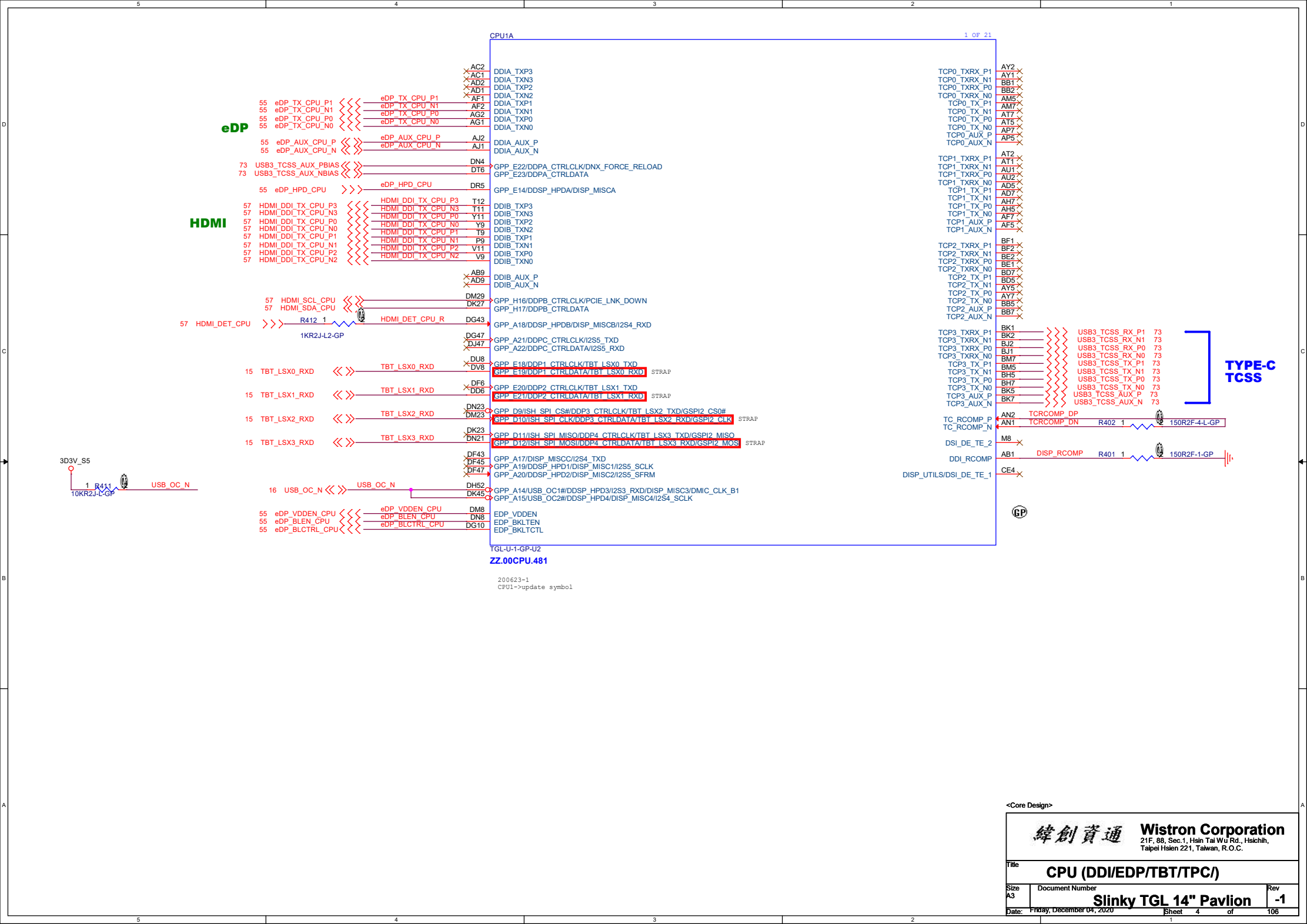
Friday, December 04, 2020

Sheet

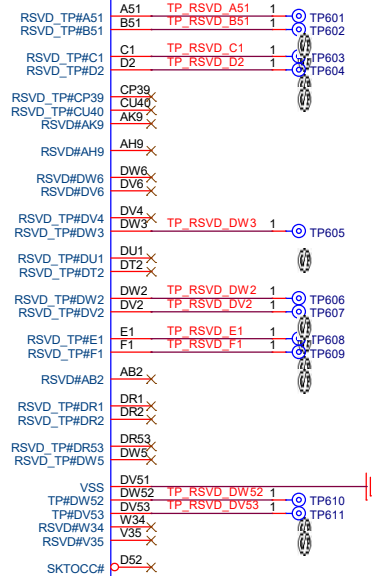
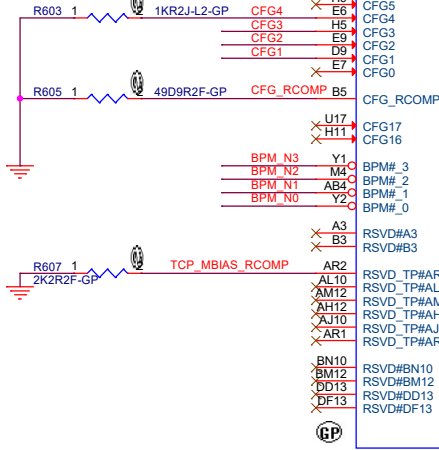
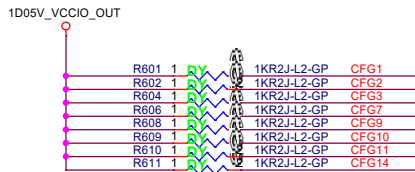
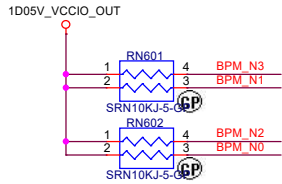
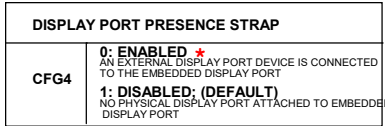
3

of

106

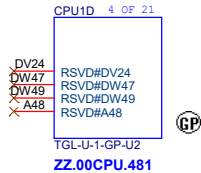
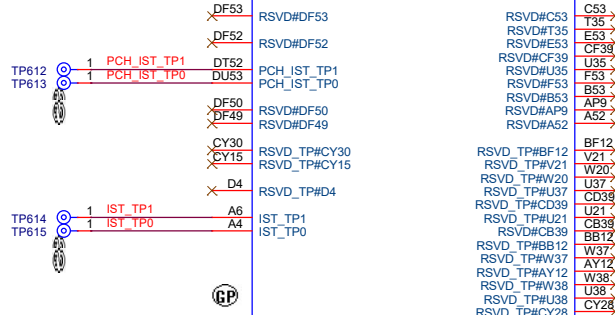






#607872 TGL PDG REV 1p0 Page114

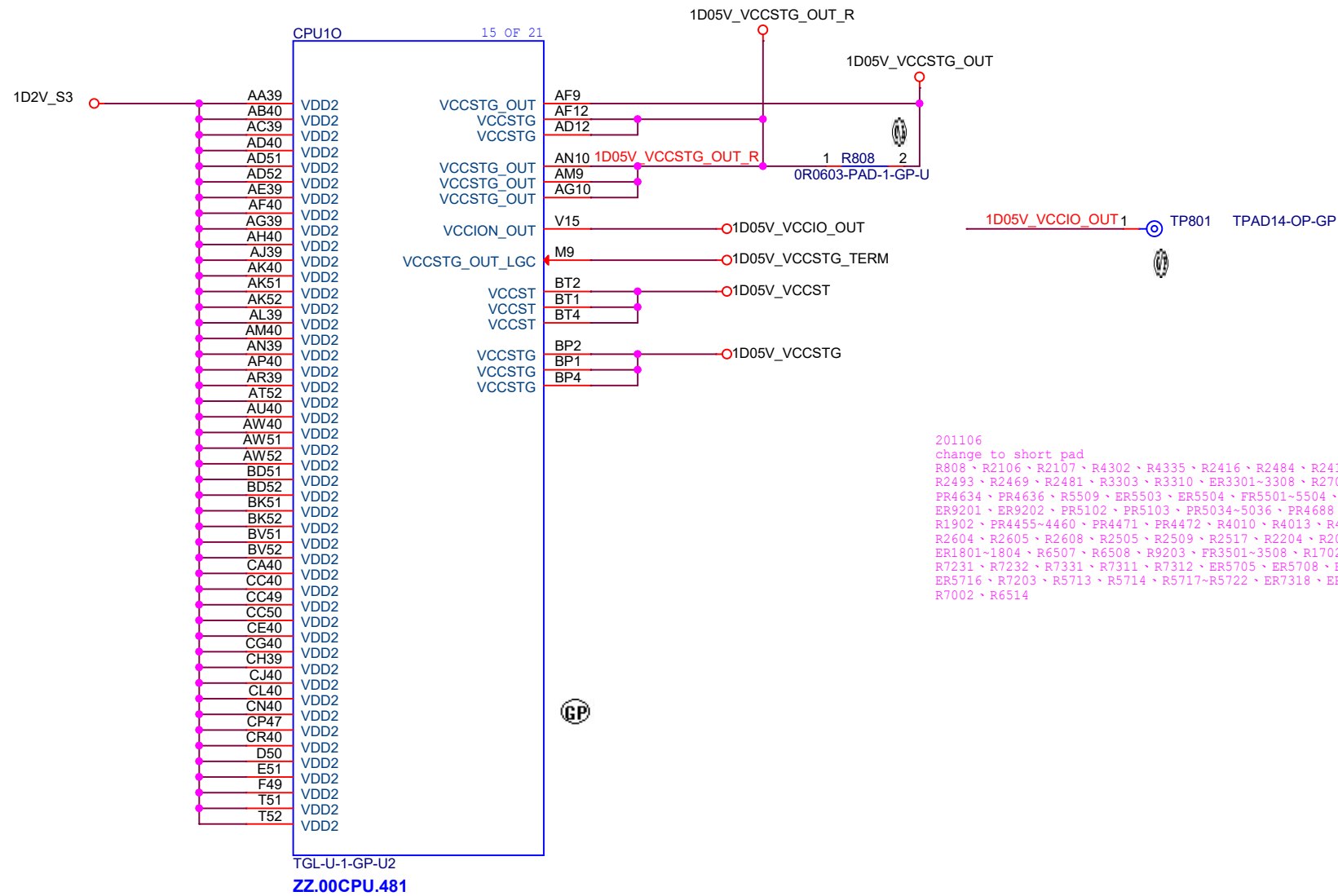
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15 ]	RSVD	None	



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Main Func = CPU



<Core Design>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>CPU (VDDQ/VCC/VCCST)</b>					
Size A4	Document Number <b>Slinky TGL 14" Pavilion</b>				Rev <b>-1</b>
Date: Friday, December 04, 2020		Sheet 8		of 106	



Reserved

<Core Design>

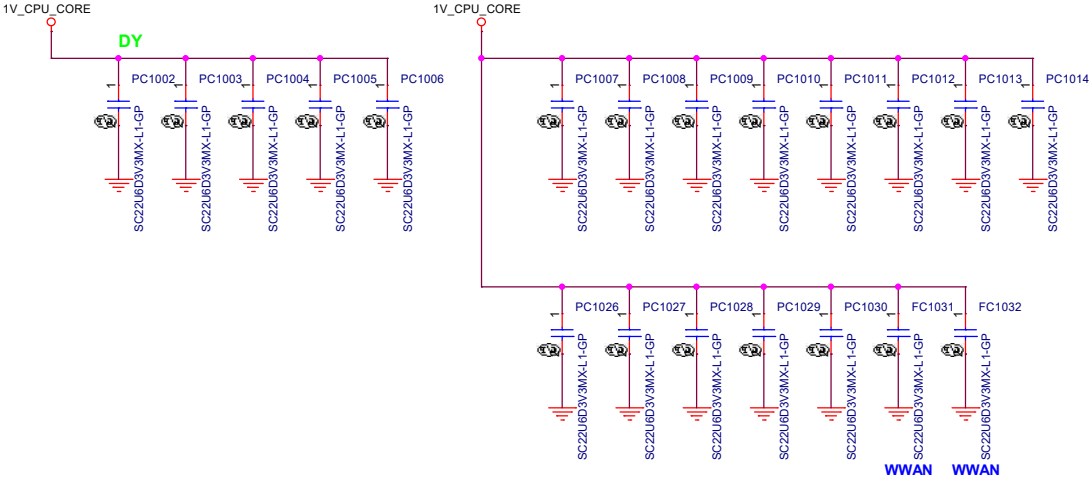
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (RSVD)			
Size	Document Number		Rev
A4	Slinky TGL 14" Pavilion		-1
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Main Func = CPU

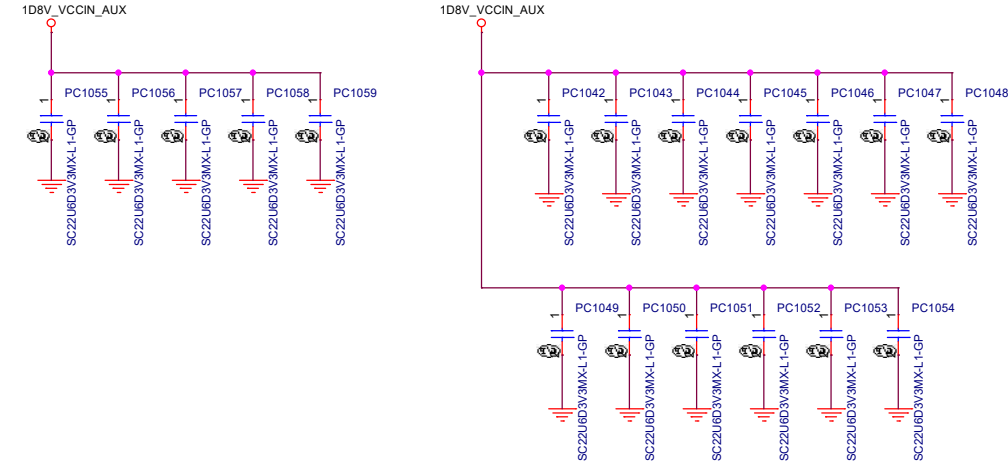
VccIN TGL\_U42

U42(15W)  
IccMax current-10ms max = 55 A

22uF	PCS	Cap
U42	13	330uF*1

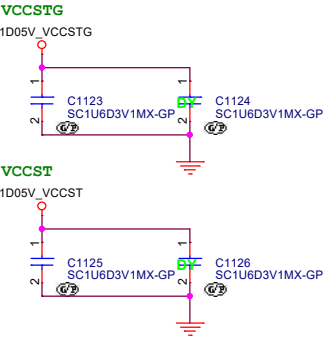
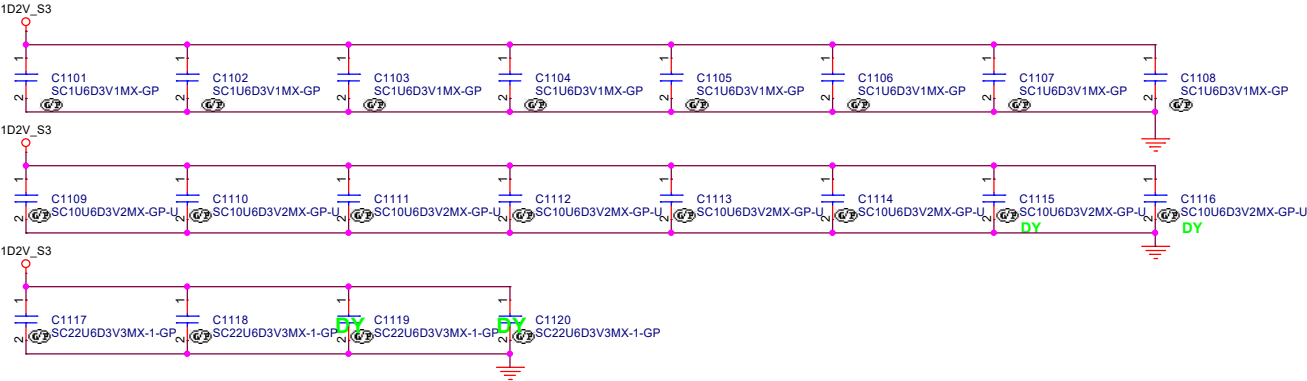


VccIN\_AUX



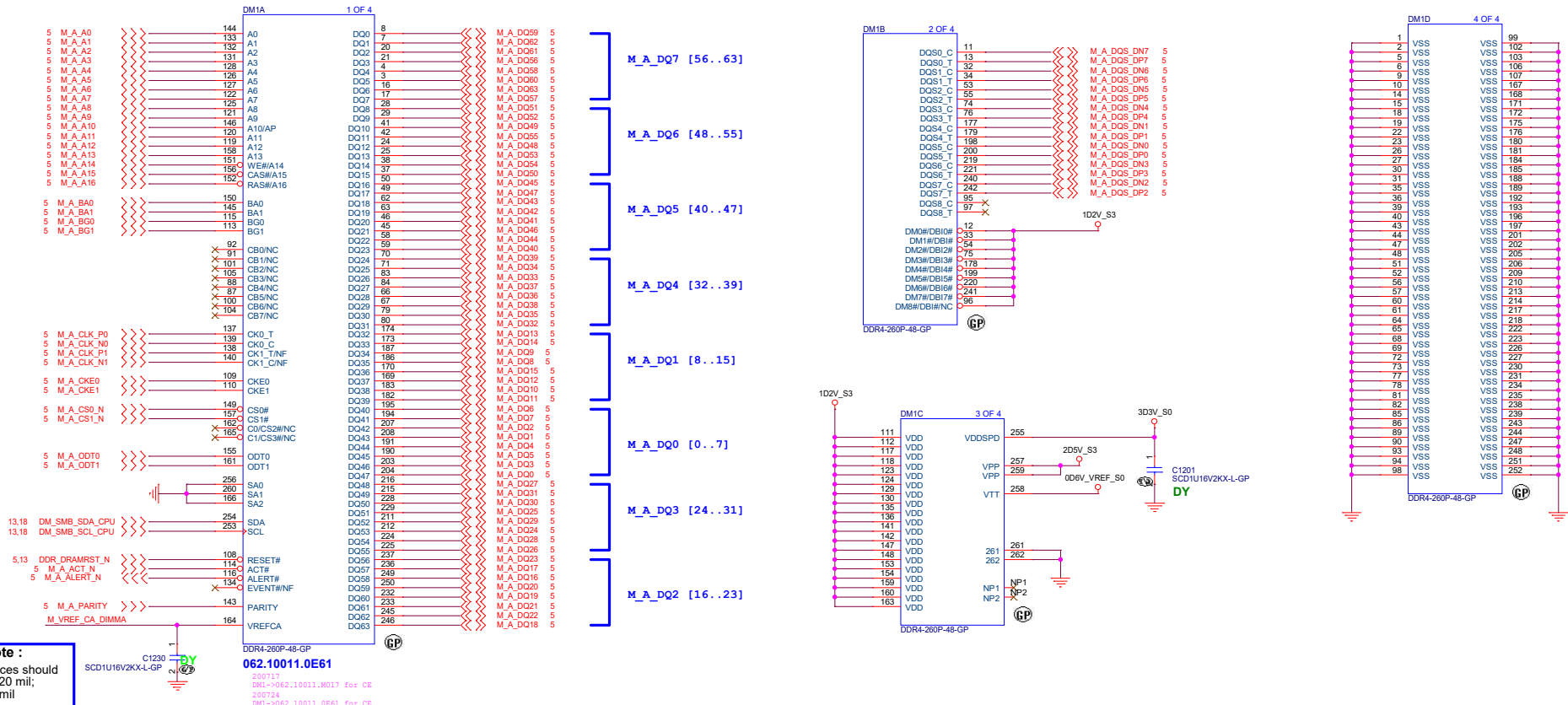
Main Func = CPU

VDDQ



## Main Func = DDR SODIMM

## DDR4 Standard Type



&lt;Core Design&gt;

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Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipai Hsein 221, Taiwan, R.O.C.

Title

012\_DDR (DDR4-CHA)

Size

Document Number

Slinky TGL 14" Pavilion

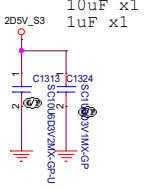
Rev

Date: Friday, December 04, 2020

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106

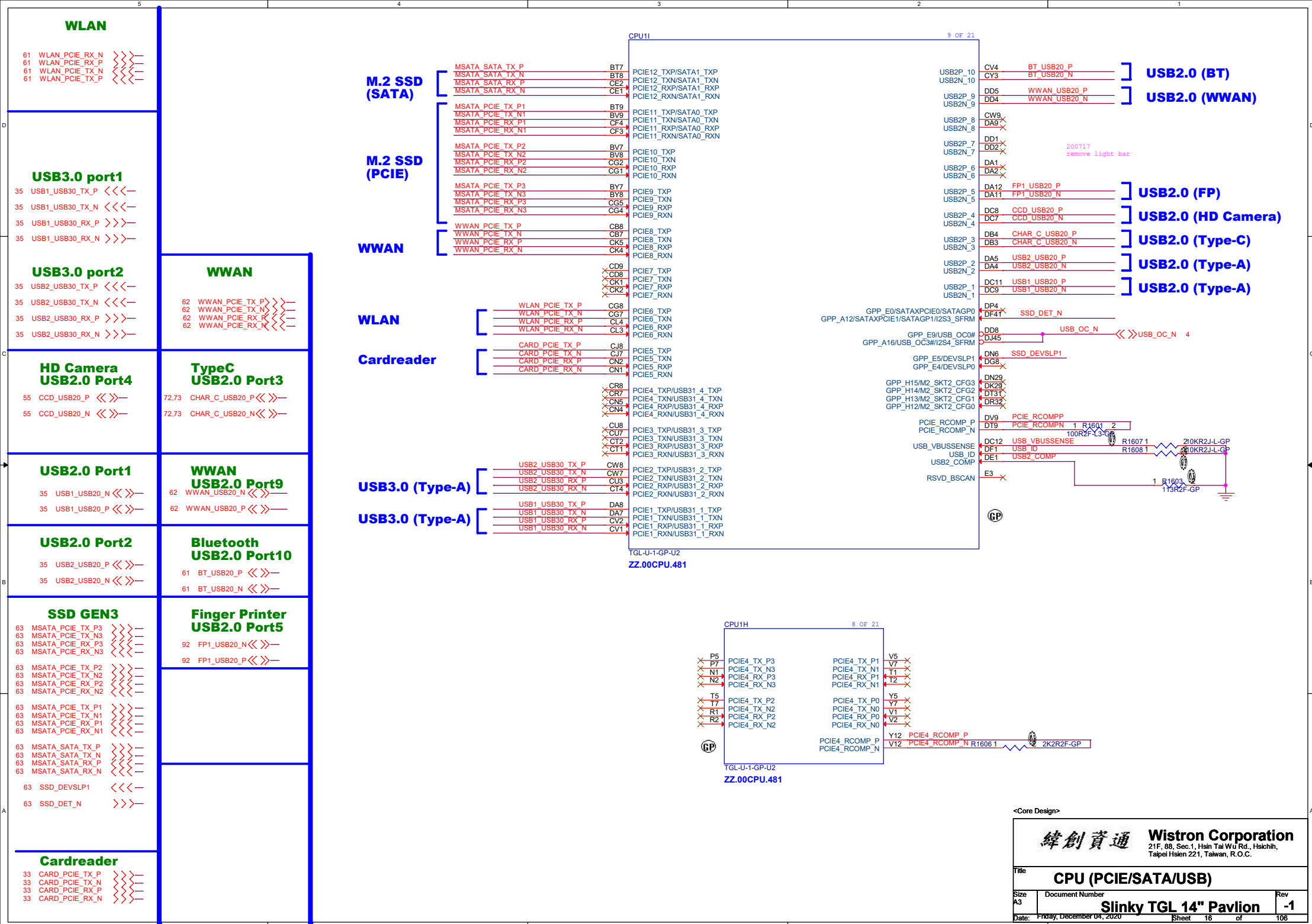
## DDR4 Reverse Type



Title			
013_DDR (DDR4-CHB)			
Size Custom	Document Number	Slinky TGL 14" Pavilion	Rev -1
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GPIO	GPP_C5	SPIO_MOSI	GPP_E6	GPP_B23	SPIO_IO2	CNV_BRI_DT	CNV_RGI_DT	TBT_LSX3_RXD
Schematic								
High	Disable	Reserved	Reserved	19.2MHZ CLOCK FROM DIVIDER (FROM INTERNAL DIVIDER)	Reserved	24M	INTEGRATED CNVI DISABLE	3.3V
Low	Enable =default=	Reserved	Reserved	38.4MHZ CLOCK DIRECT FROM CRYSTAL (DEFAULT) =default=	Reserved	38.4M =default=	INTEGRATED CNVI ENABLE	1.8V
GPIO	GPP_B18/GSPI0_MOSI	HDA_SDO	TBT_LSX #0	TBT_LSX #1	TBT_LSX #2	GPD7	SPIO_IO3	GPP_C2
Schematic								
High	Enable	Disable	3.3V	3.3V	3.3V	Reserved	Reserved	Enable
Low	Disable =default=	Enable =default=	1.8V	1.8V	1.8V	Reserved	Reserved	Disable =default=
GPIO	GPP_H2		ITP_PMODE		GPP_E10	GPP_E11		
Schematic								
High	1 = Slave Attached Flash Sharing (SAFS) is enabled.		Reserved					
Low	0 = Master Attached Flash Sharing (MAFS) is enabled. (Default)		Reserved					

<Core Design>







TPM  
EC and Flash ROM

OTHER

SMBus

WLAN

SSD

Cardreader

ESPI

WWAN

Cardreader

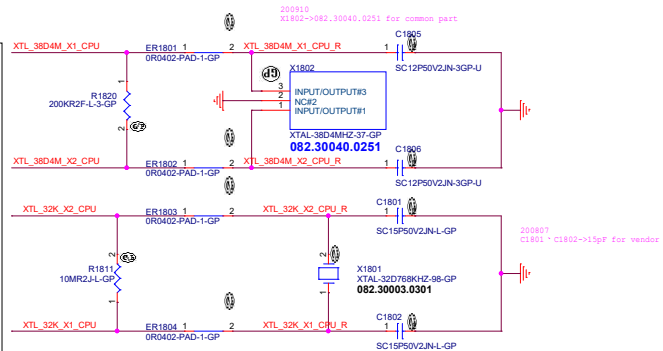
WLAN

WWAN

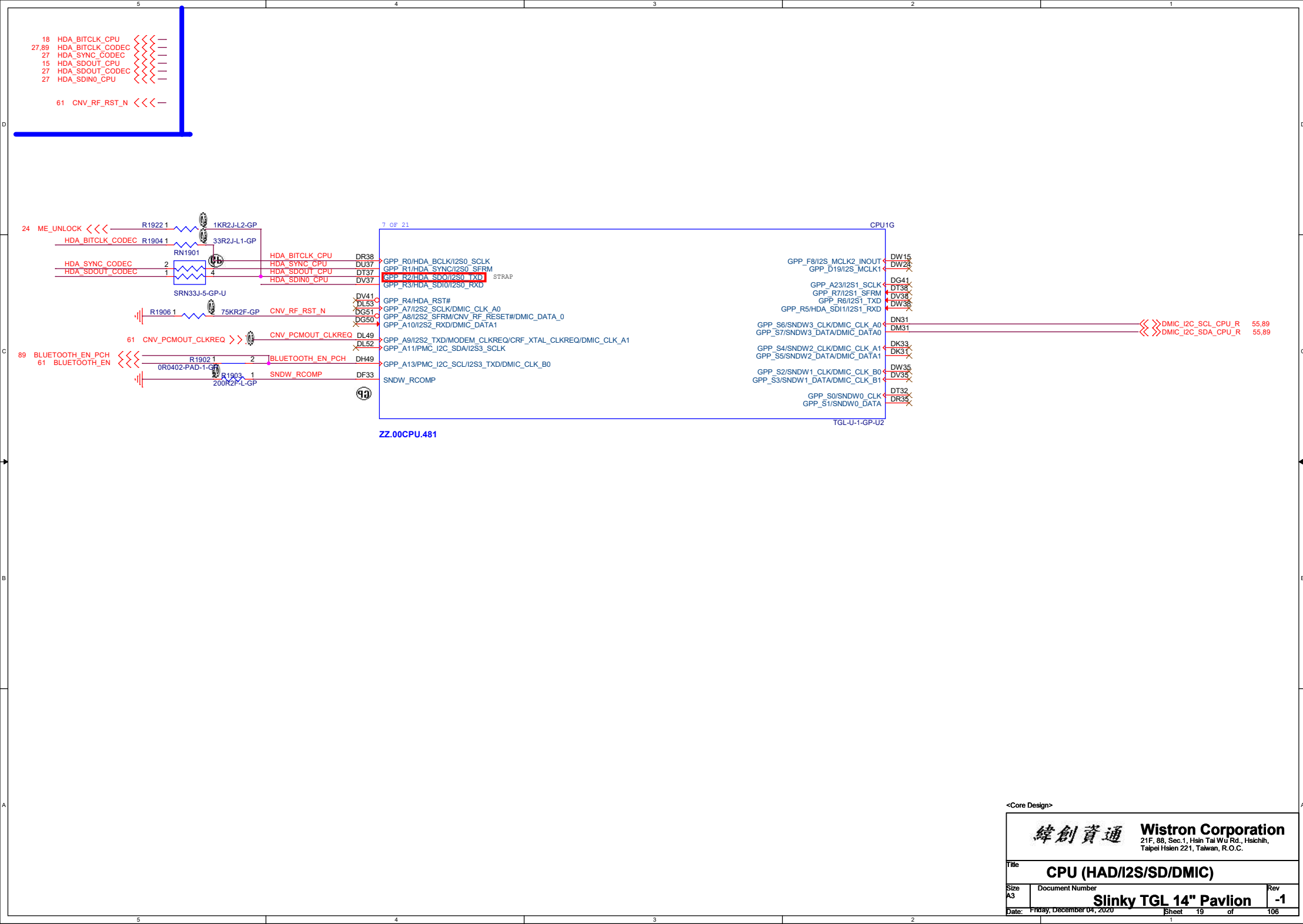
SSD

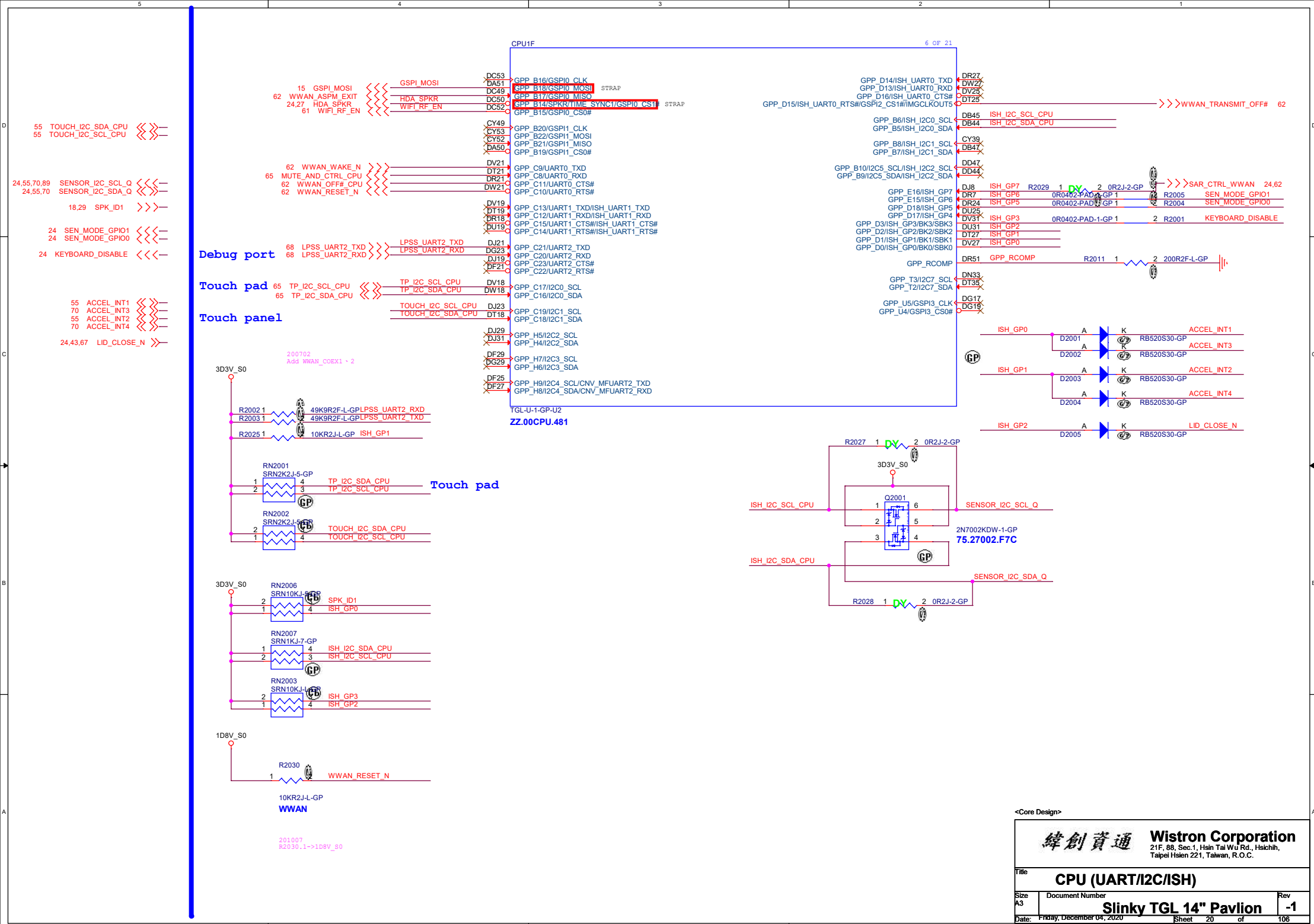
SSD PCIE GEN 4

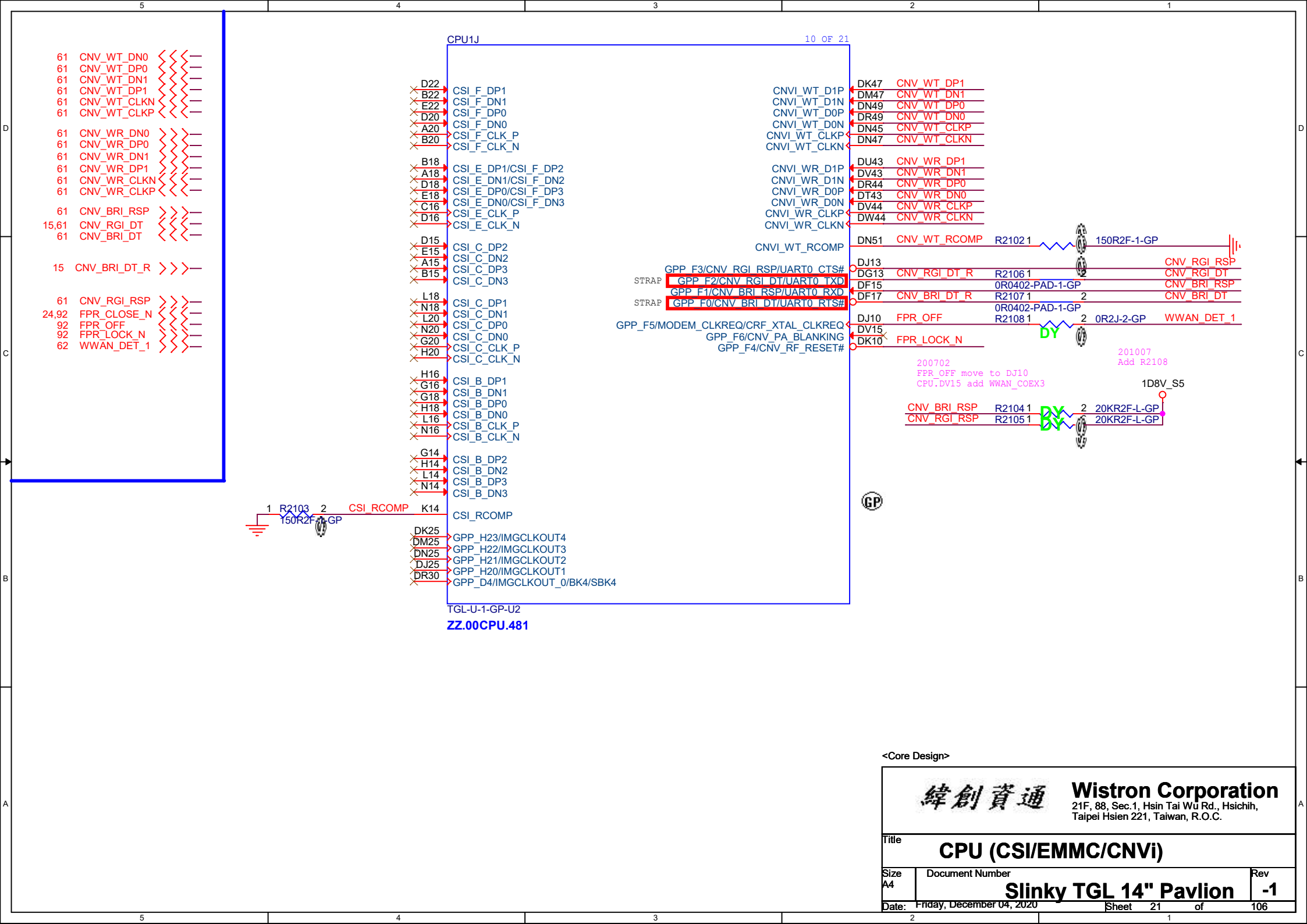
RTC Reset



<Core Design>







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (CSI/EMMC/CNVi)

Size  
A4

Document Number

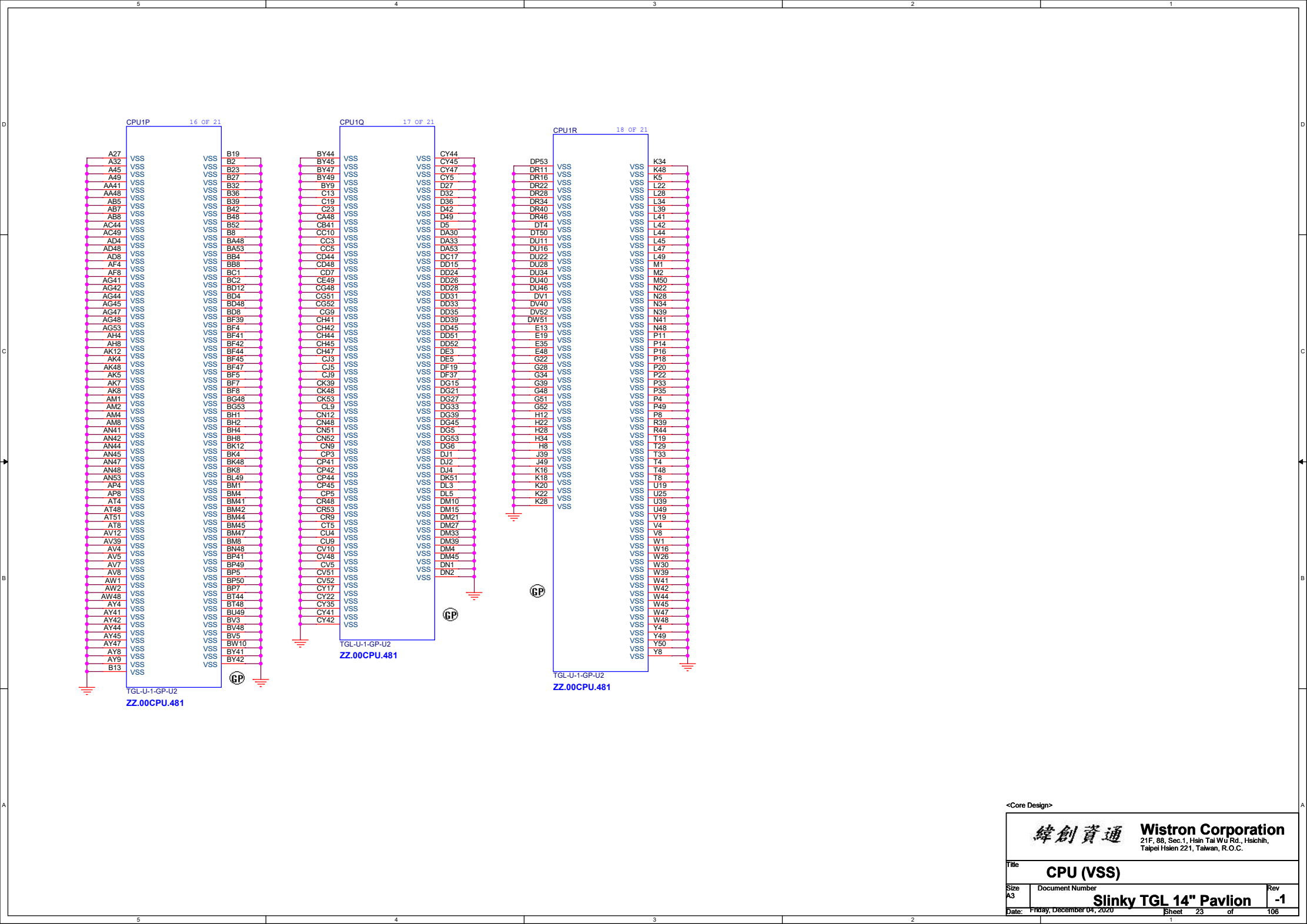
Slinky TGL 14" Pavilion

Rev  
-1

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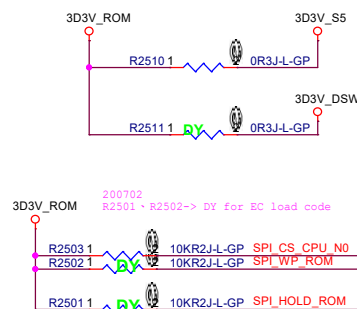
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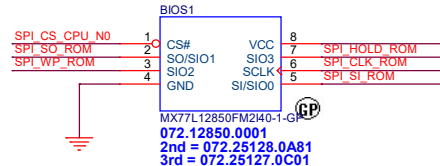
## SSID = Flash.ROM

18,24 SPI\_CS\_CPU\_N0  
18 SPI\_SO\_ROM  
18 SPI\_WP\_ROM  
18 SPI\_HOLD\_ROM  
18 SPI\_CLK\_ROM  
18 SPI\_SI\_ROM



200731 Reserve power domain

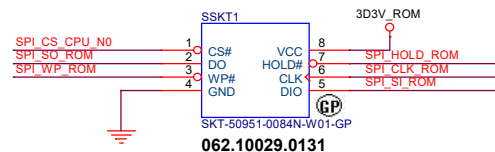
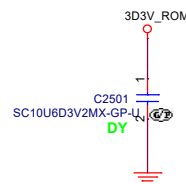
## RPMC



200717 BIOS1 -> 072.12850.0001

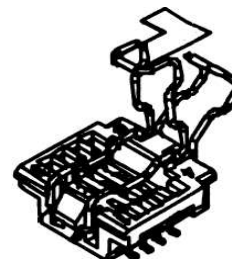
2020.05.18 ALL BIOS POWER DOMAIN CHANGE FROM 3D3V\_DSW TO 3D3V\_S5 (AUTO LOADCODE ISSUE)

## SPI FLASH ROM 16M byte

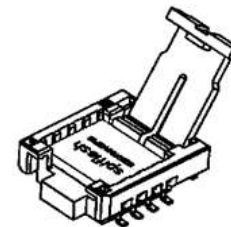


200717 SSKT1 -> 062.10029.0131

Co-lay with BIOS1



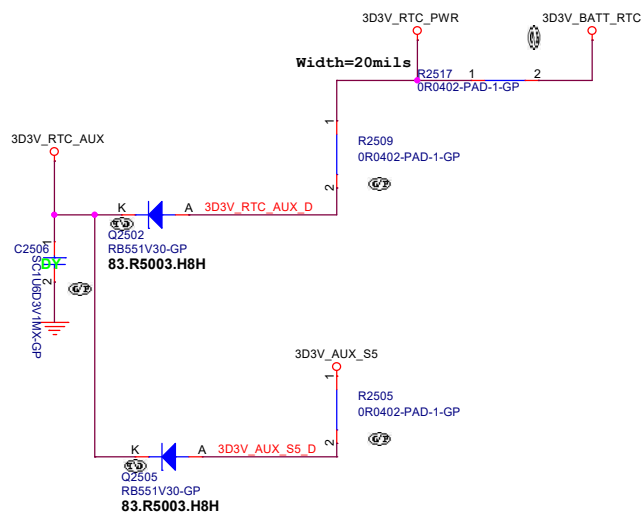
62.10089.011



062.10029.0131

V

## SSID = RBAT



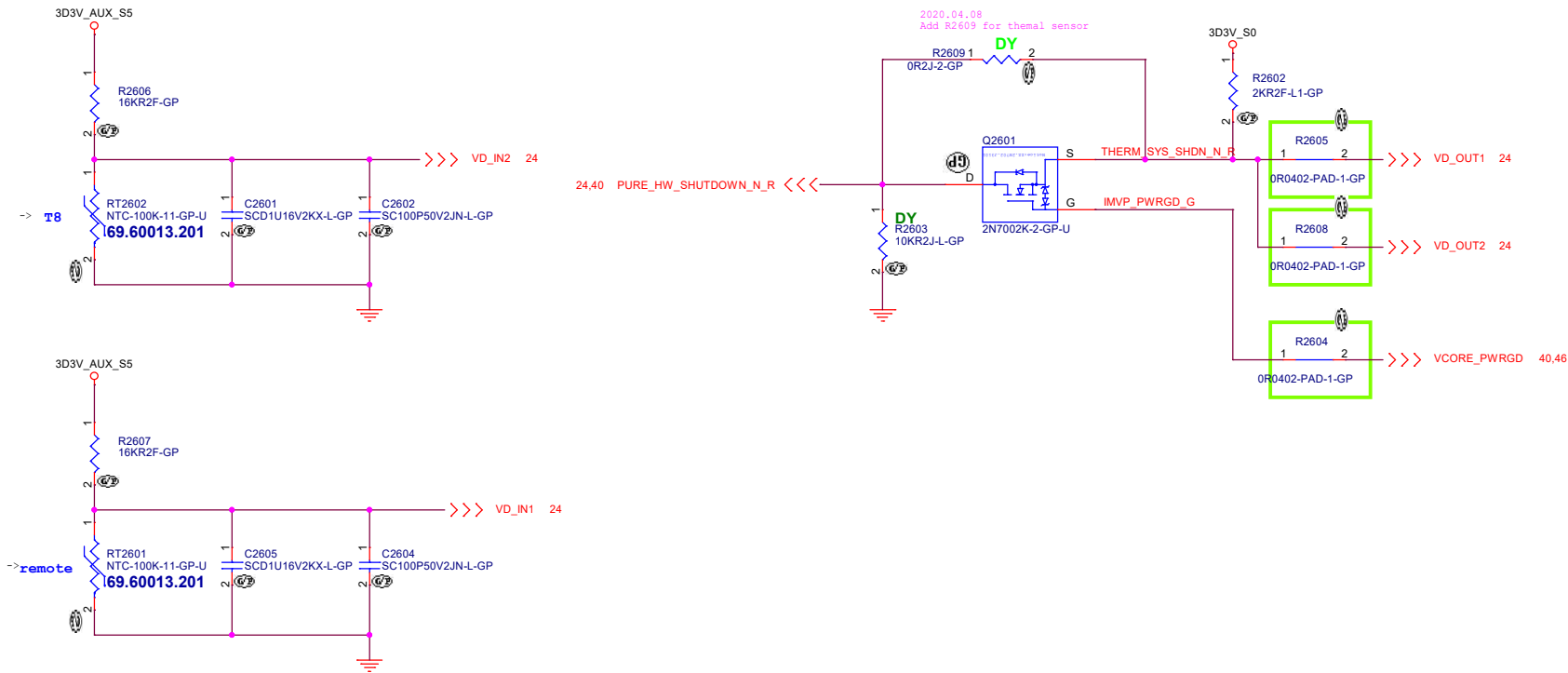
<Core Design>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	Flash/RTC
Size A3	Document Number
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<b>Slinky TGL 14" Pavilion</b> Rev -1	



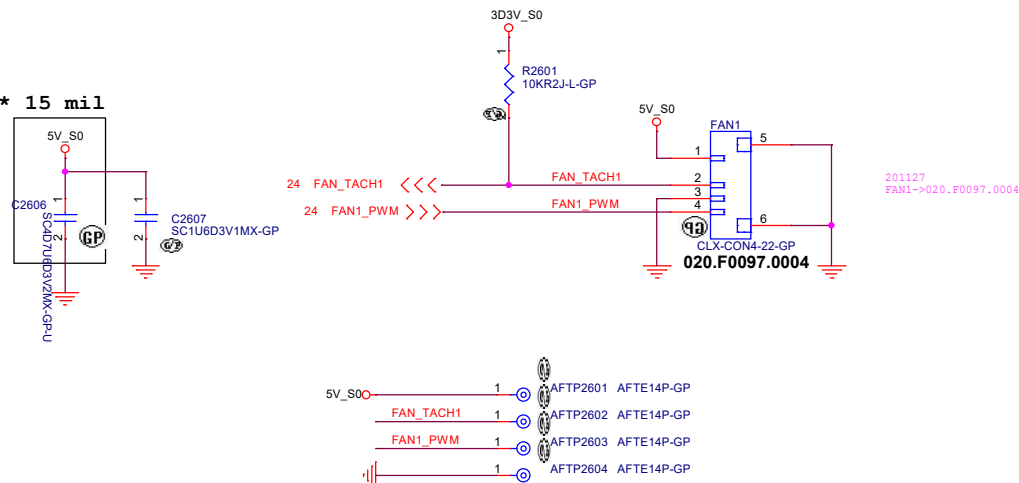
SSID = Thermal

## Thermal sensor NCT 7718W



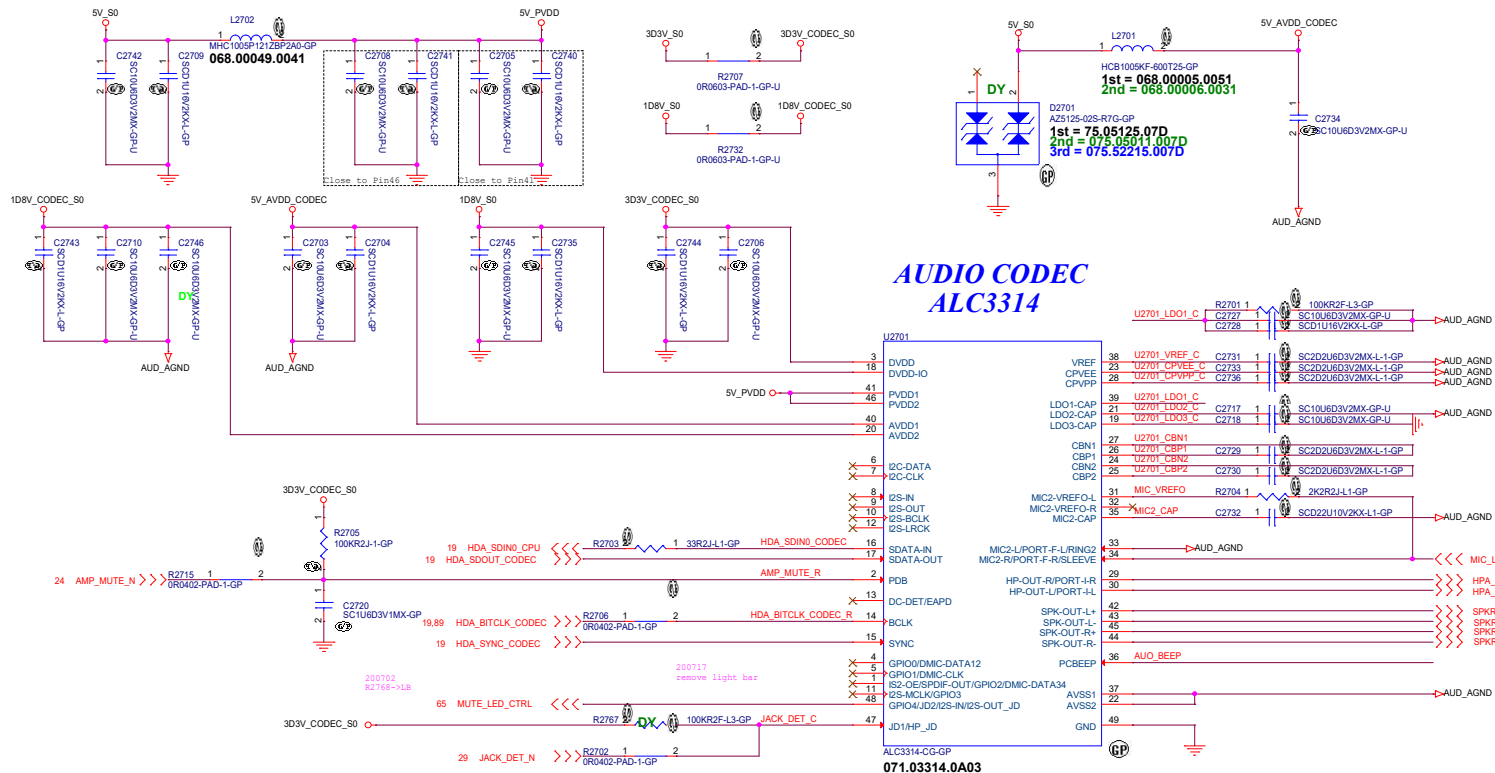
## Fan Conn

\*Layout\* 15 mil



<Core Design>

SSID = AUDIO

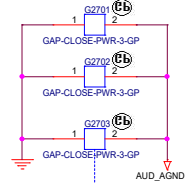


Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-  
Speaker 4 ohm : 40mil  
Speaker 8 ohm : 20mil

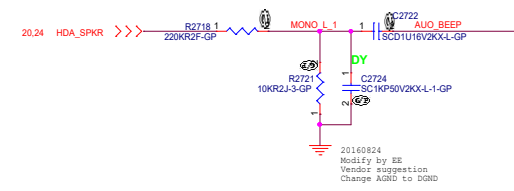
## AMP. for Headphone

## Digital GND & AUD\_AGND

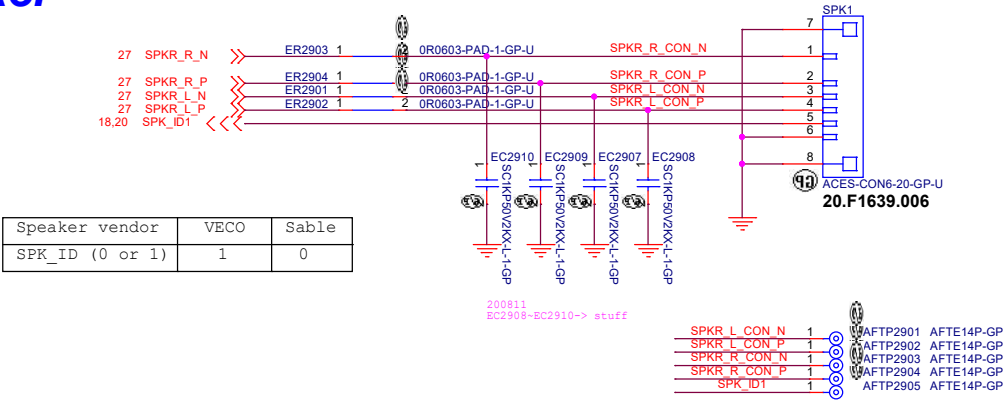
Tie Analog GND and Digital GND under codec by a single point



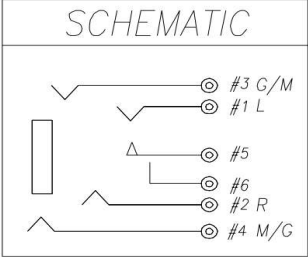
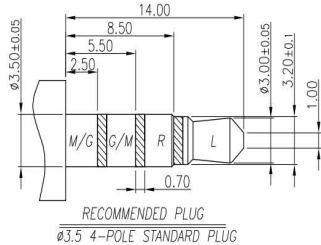
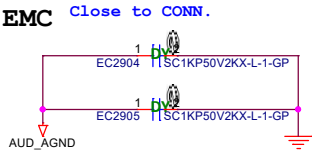
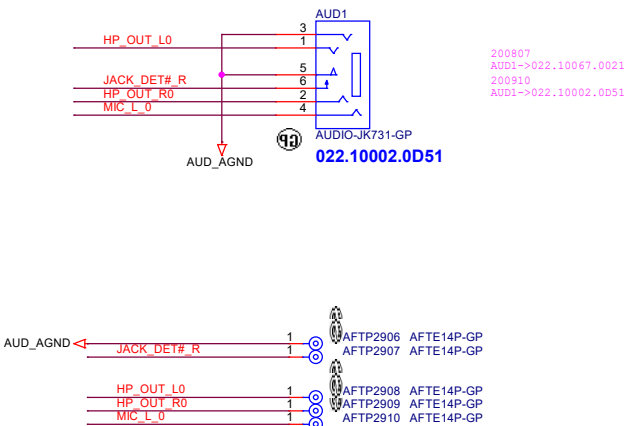
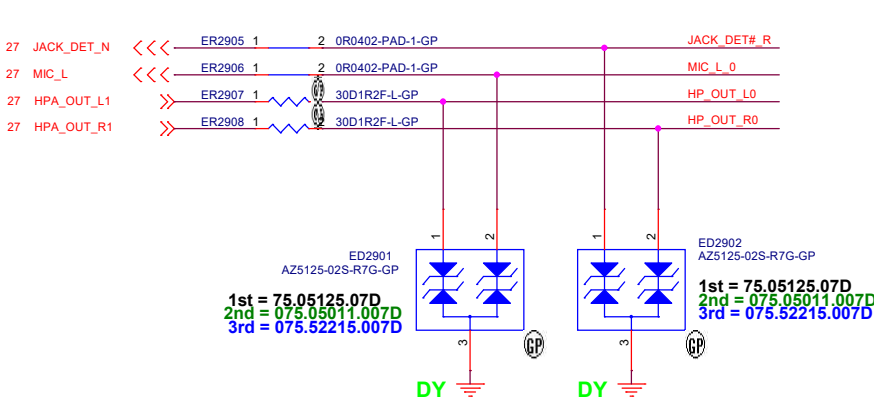
## PC BEEP



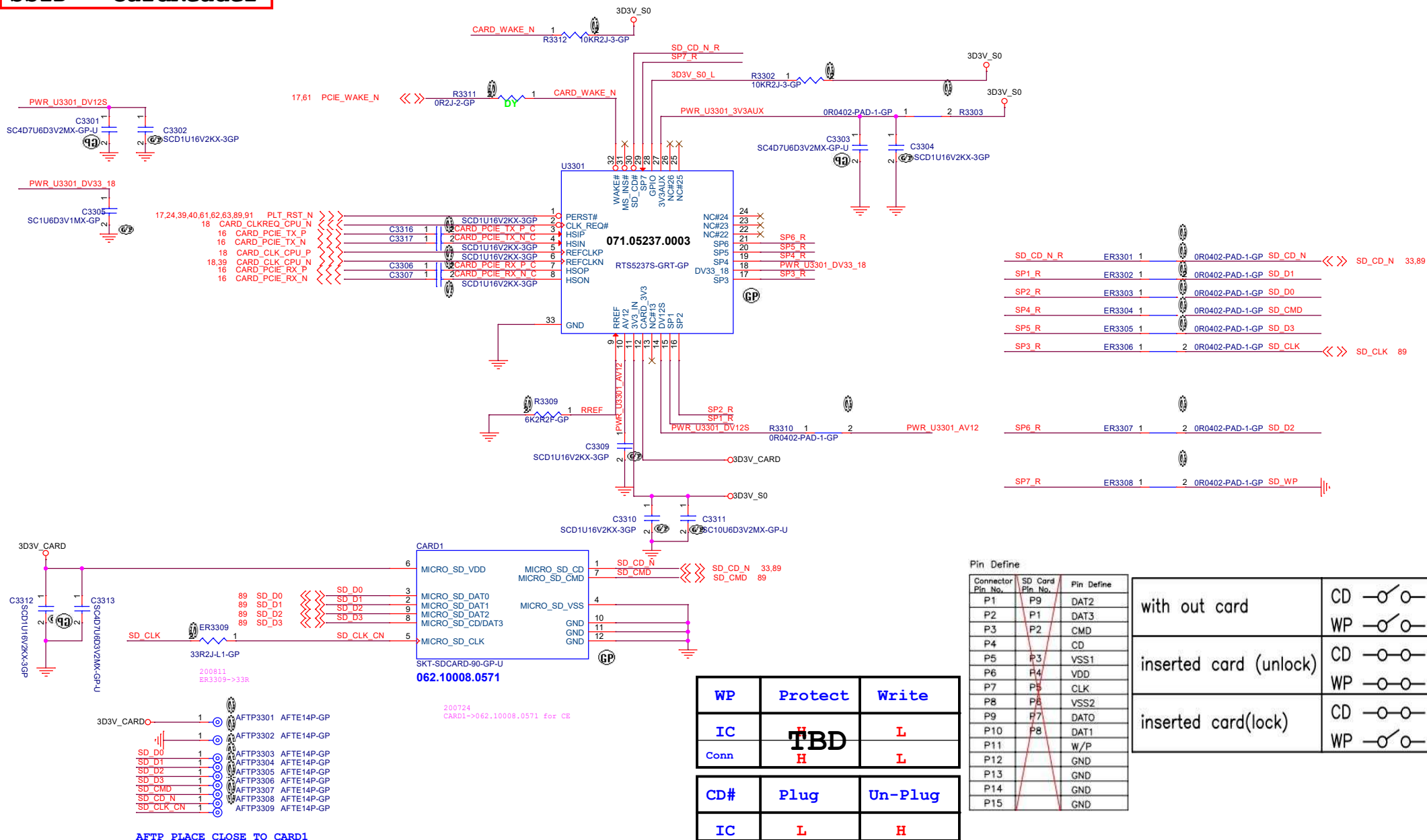
Speaker



Audio\_Combo\_Jack



```
SSID = CardReader
```









WP	Protect	Write
IC	<b>TBD</b>	L
Conn	H	L

CD#	Plug	Un-Plug
IC	L	H
Conn	L	H

Pin Define		
Connector Pin No.	SD Card Pin No.	Pin Define
P1	P9	DAT2
P2	P1	DAT3
P3	P2	CMD
P4		CD
P5	P3	VSS1
P6	P4	VDD
P7	P5	CLK
P8	P6	VSS2
P9	P7	DAT0
P10	P8	DAT1
P11		W/P
P12		GND
P13		GND
P14		GND
P15		GND

with out card	CD  CD WP  WP
inserted card (unlock)	CD  CD WP  WP
inserted card(lock)	CD  CD WP  WP

### <Core Design>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title:

**CARDREADER (SDIO/SD Conn)**

Size

Document Num	
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**Slinky TGL 14" Pavlion**

Rev

Date: Friday, December 04, 2020

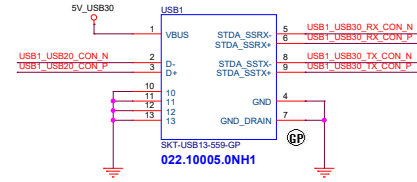
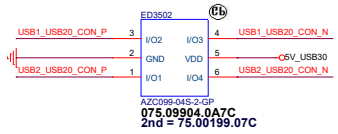
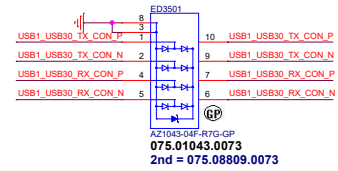
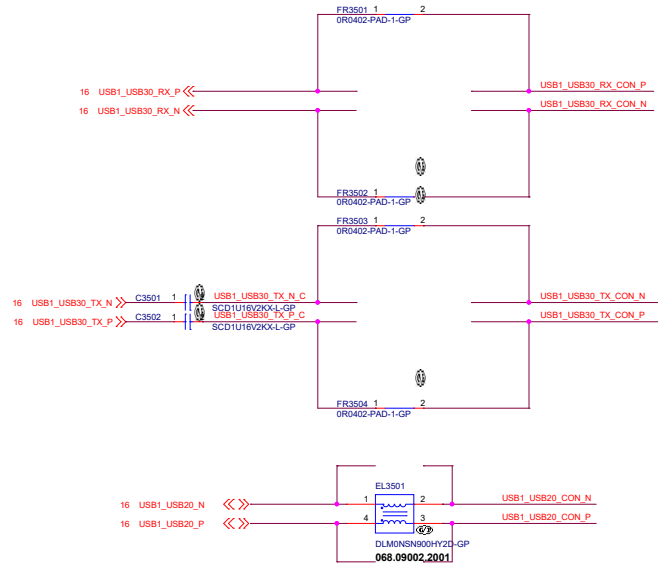
She

3:

24

106

## USB Type A Connector

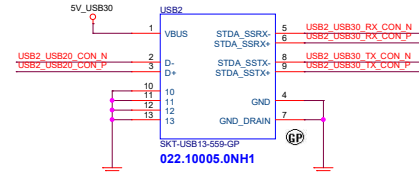
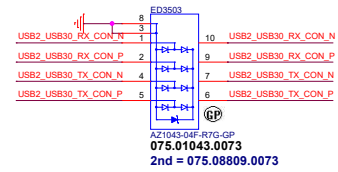
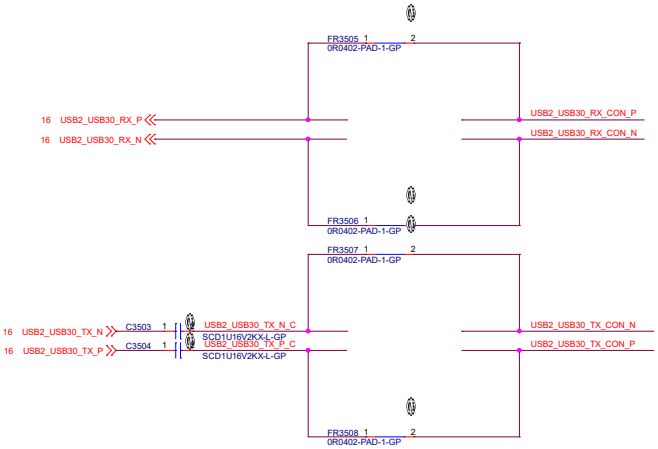


AFTP PLACE CLOSE TO USB1

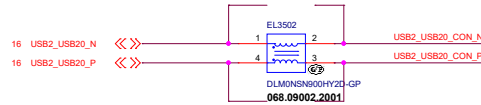


200807  
USB1、USB2->022.10005.0NH1

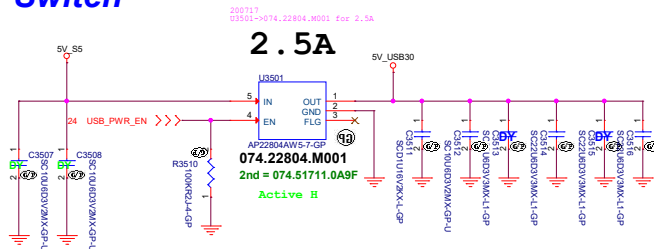
## USB Type A Connector

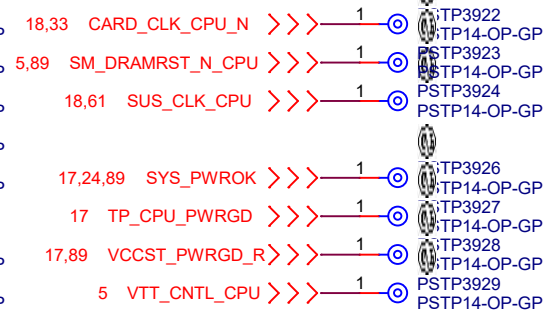
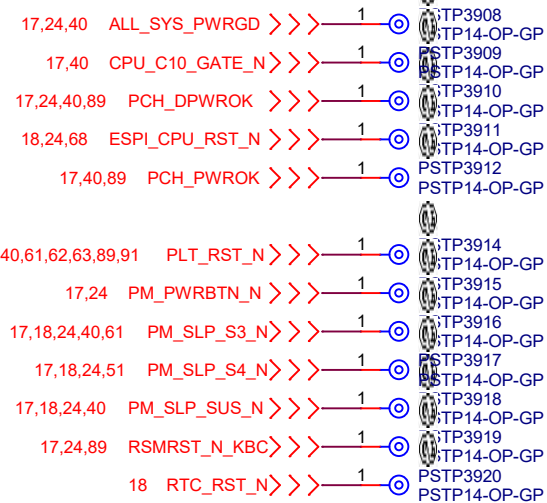
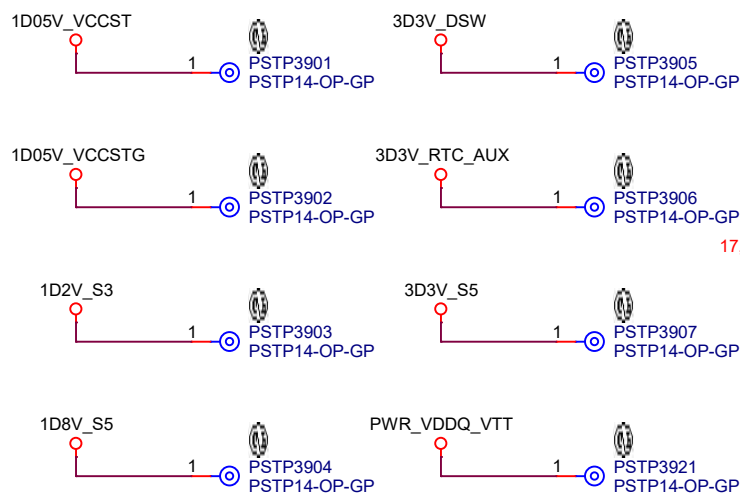


AFTP PLACE CLOSE TO USB2



## Power Switch





201001  
Del PSTP3925、PSTP3913

200724  
PSTP3901~3929->ZZ.PAD02.561

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緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Sequence (RSVD)**

Size  
A4

Document Number

Rev

**Slinky TGL 14" Pavilion**

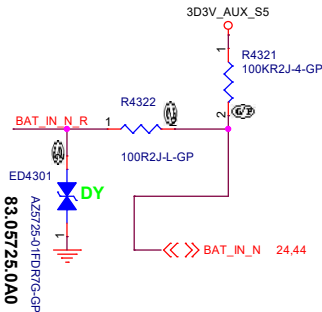
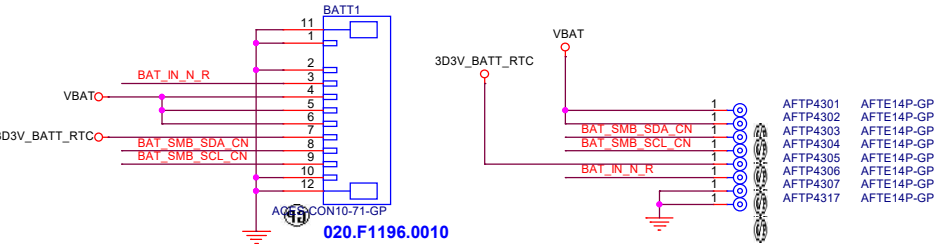
**-1**

Date: Friday, December 04, 2020

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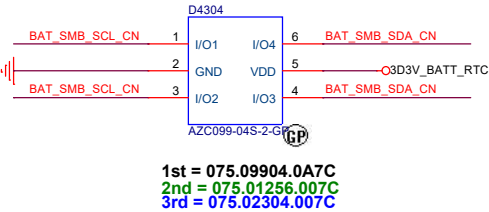


Battery Conn

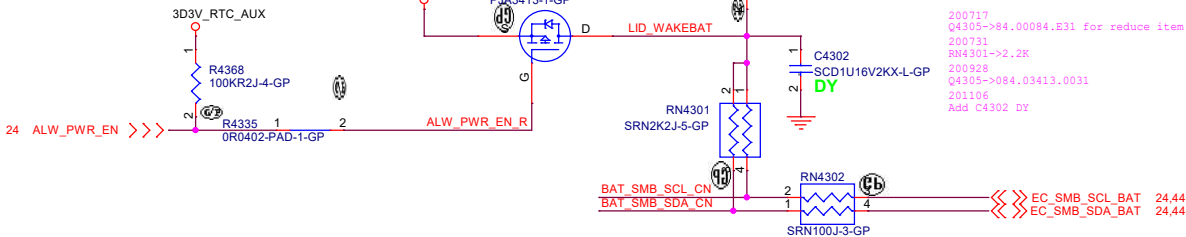
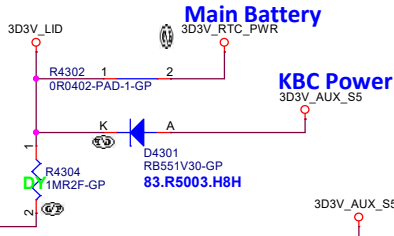


3. Interface  
Connector : 10pin

Pin No.	Symbol	Description
1,2	GND	Batt-, Battery Negative Terminal
3	B/I	Connected to GND.
4,5,6	BATT+	Batt+, Battery Positive Terminal.
7	RTC	3.3V (see Note 7)
8	SMD	SMBus data interface I/O pin.
9	SMC	SMBus clock interface I/O pin
10	GND	Batt-, Battery Negative Terminal

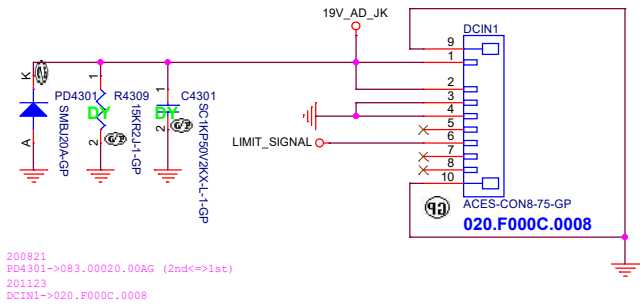
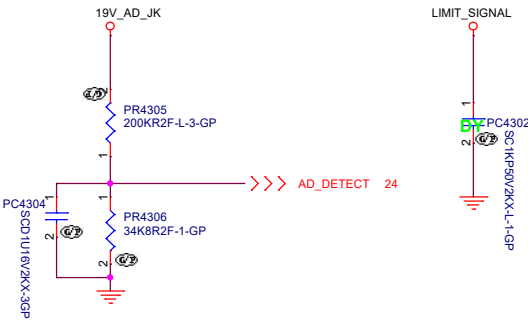


1st = 075.09904.0A7C  
2nd = 075.01256.007C  
3rd = 075.02304.007C

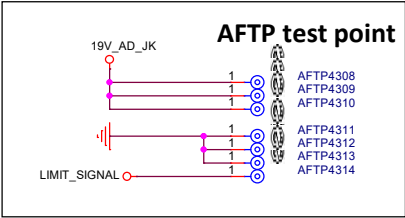


200717 Q4305->84.00084.E31 for reduce item  
200731 RN4301->2.2K  
200928 Q4305->084.03413.0031  
201106 Add C4302 DY

DCIN JACK



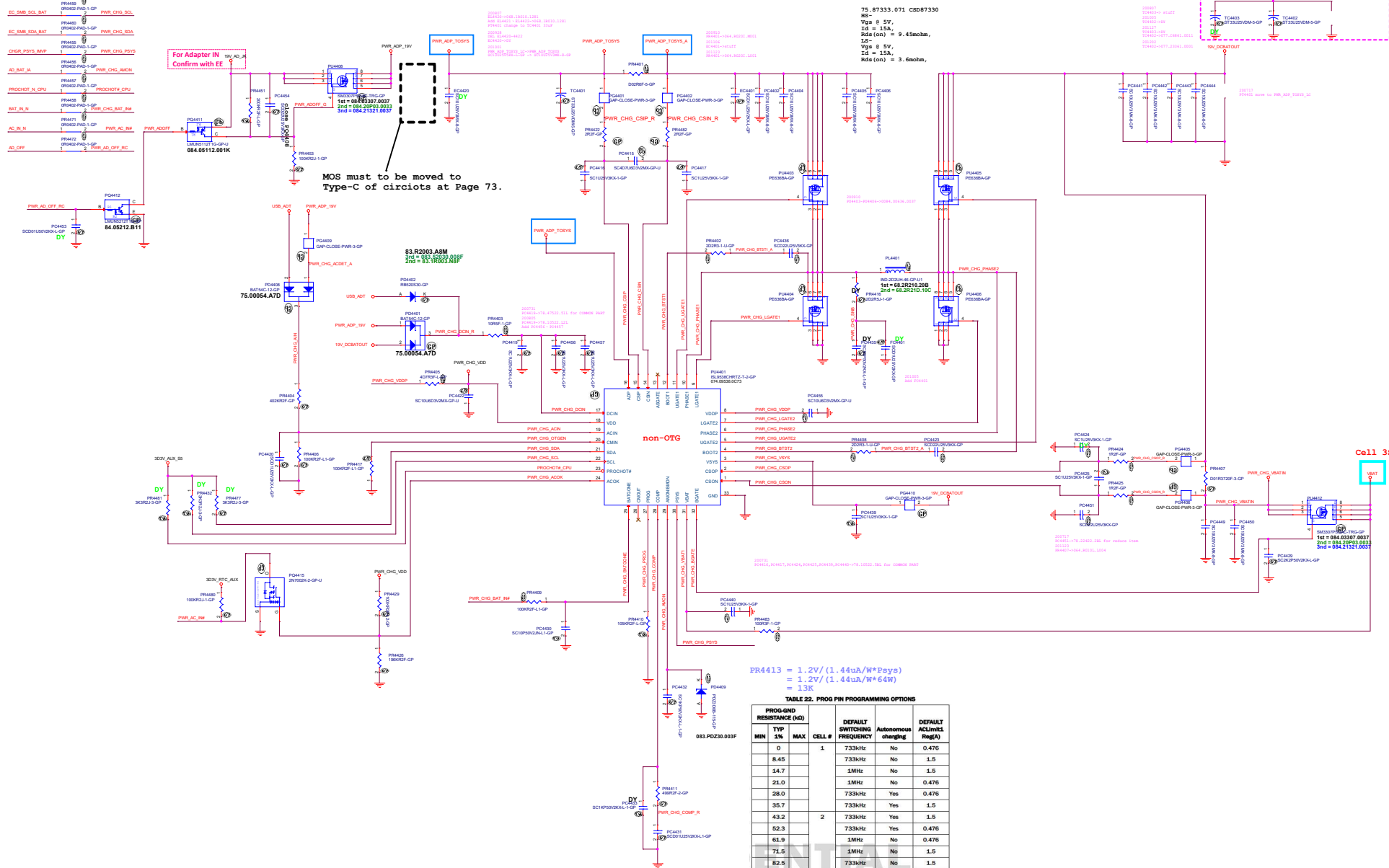
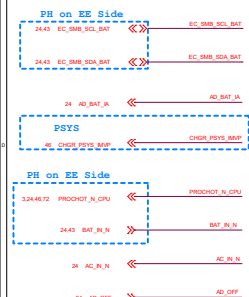
200821 PD4301->083.00020.00AG (2nd<=>1st)  
201123 DCIN1->020.F000C.0008





## OFFPAGE

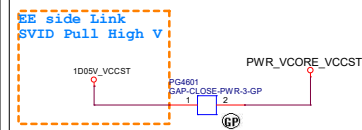
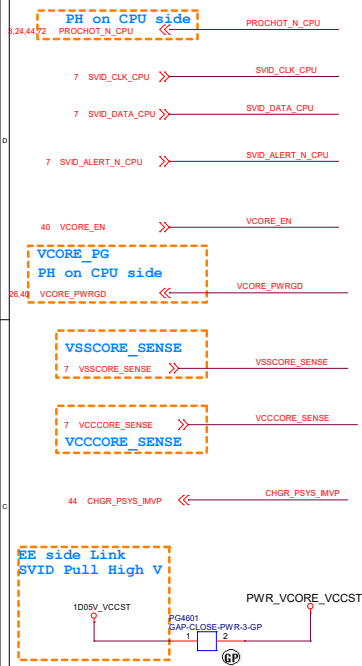
**Main Func = Charger**



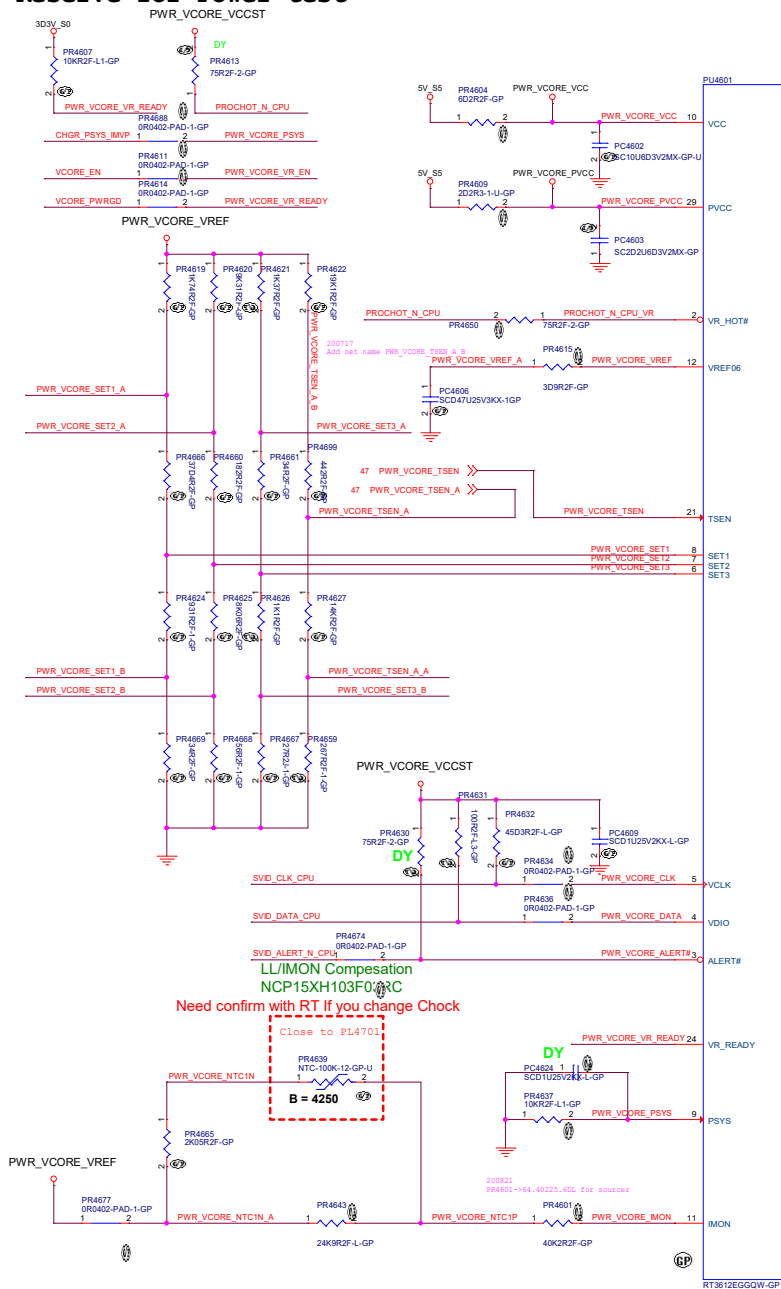
PROG-GND RESISTANCE (kΩ)		CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLM1RegA RegA
MIN	MAX				
0		1	733kHz	No	0.476
8.45			733kHz	No	1.5
14.7			1MHz	No	1.5
21.0			1MHz	No	0.476
28.0			733kHz	Yes	0.476
35.7			733kHz	Yes	1.5
43.2		2	733kHz	Yes	1.5
52.3			733kHz	Yes	0.476
61.9			1MHz	No	0.476
71.5			1MHz	No	1.5
82.5			733kHz	No	1.5
93.1			733kHz	No	0.476
105		3	733kHz	No	0.476
118			733kHz	No	1.5
133			1MHz	No	1.5
147			1MHz	No	0.476
162			733kHz	Yes	0.476
178			733kHz	Yes	1.5
196		4	733kHz	Yes	1.5
215			733kHz	Yes	0.476
237			1MHz	No	0.476
261			1MHz	No	1.5
287			733kHz	No	1.5
316			733kHz	No	0.476
348		1	733kHz	No	0.476



## OFFPAGE



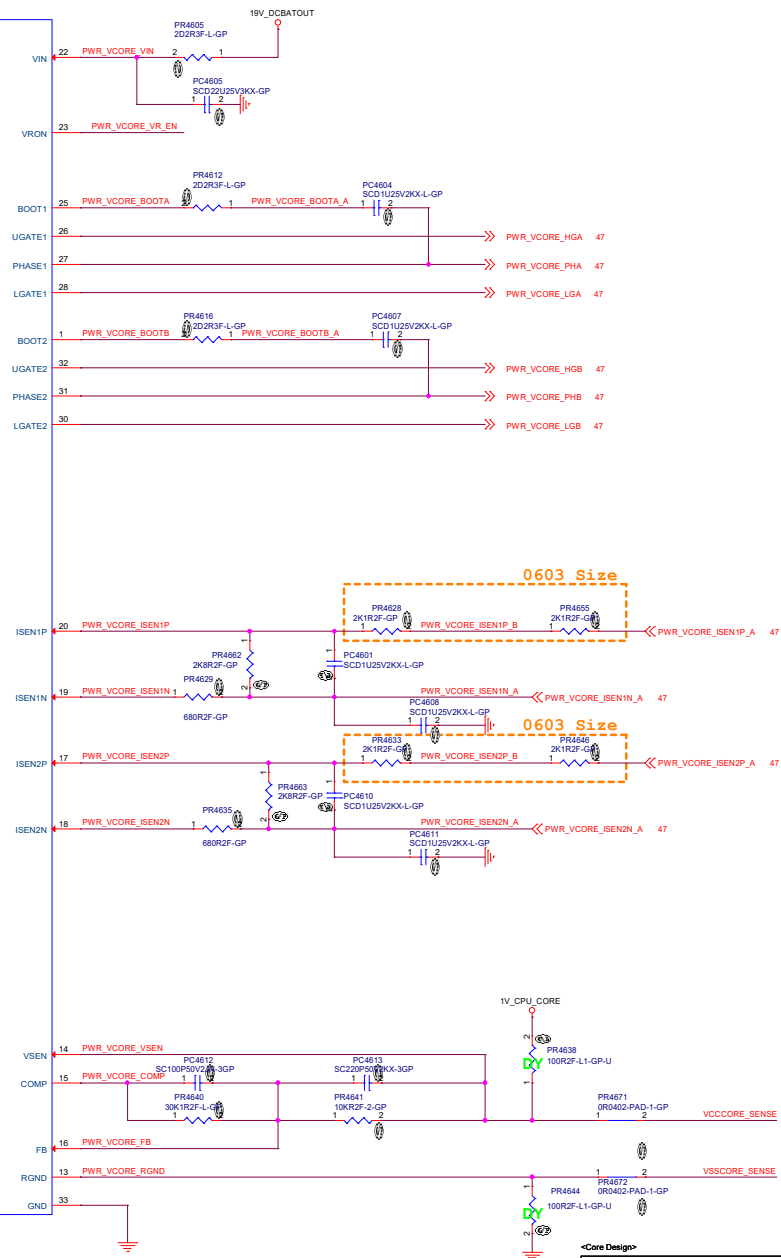
## Reserve for Power test



```

200717
Add U22 and U42 for power team request
200821
Add power change list
200910
FU4601->074.03612.0C73
200910
Remove U22 location

```



&lt;Core Design&gt;

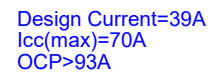
緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

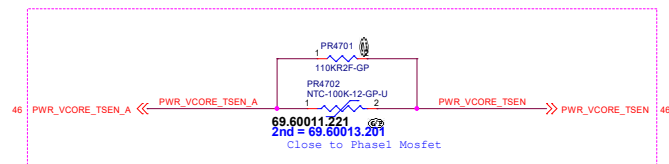
Title	<b>046 Power ISL95859 CPU VCORE</b>		
Size	Document Number	Rev	-1
Custom	<b>Slinky TGL 14" Pavilion</b>		
Date	Friday, December 04, 2020	Sheet 46 of	106



200811  
Del PG4702-05、PG4708-11  
200813  
Add FB4701-4706、FL4701-4706



PANASONIC  
ESR: 9 mohm



&lt;Core Design&gt;

Main Func = CPU\_CORE

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
048 Power_CSD97396_CPU_VCCGT		
Size	Document Number	Rev
K2	Slinky TGL 14" Pavilion	-1
Date: Friday, December 04, 2009		
Sheet 48 of 108		

PH on CPU side  
-----

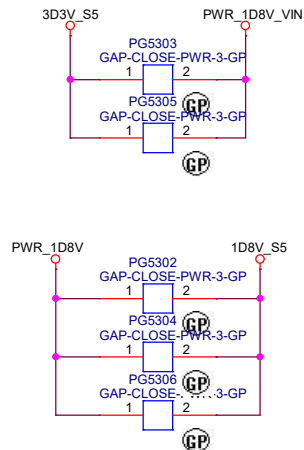


PH on CPU side  
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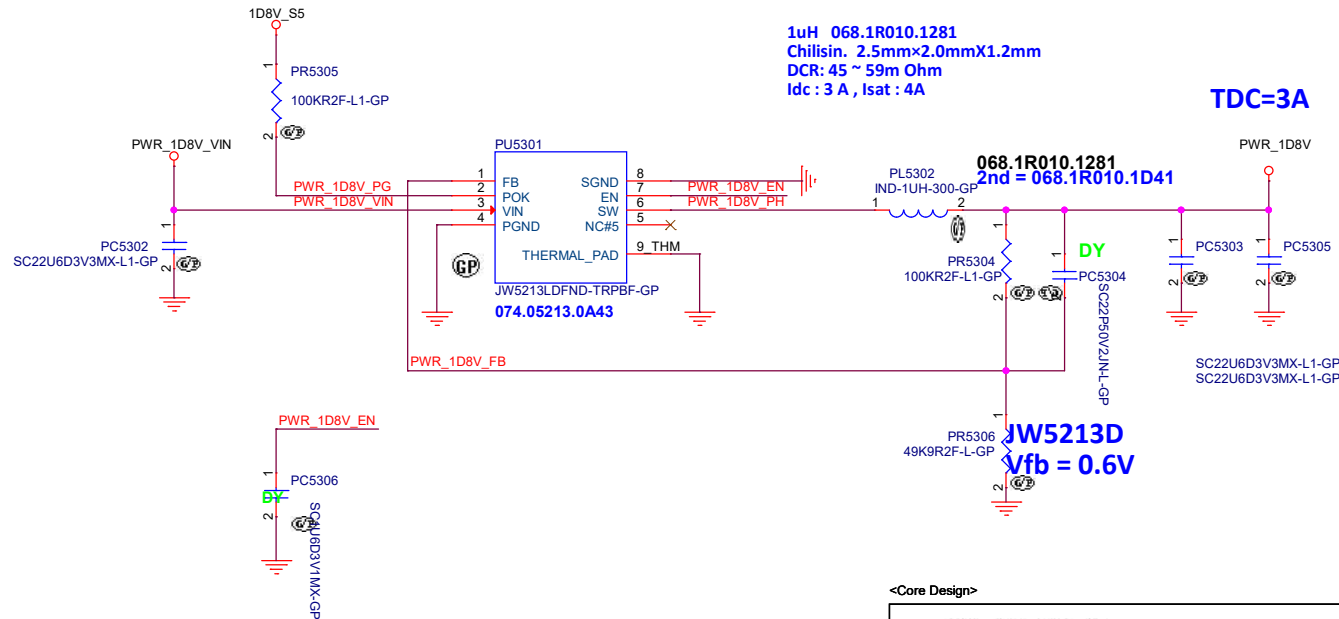




PWR\_1D8V\_EN >> PWR\_1D8V\_EN



**JW5213D\_1D8V**



### <Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
10. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	136-150

**JW5213D 1D8V**

Size  
Custom

Document Number

Rev

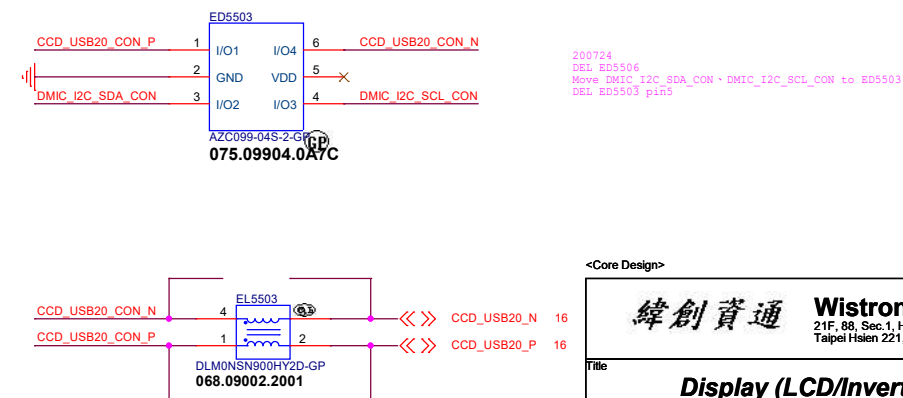
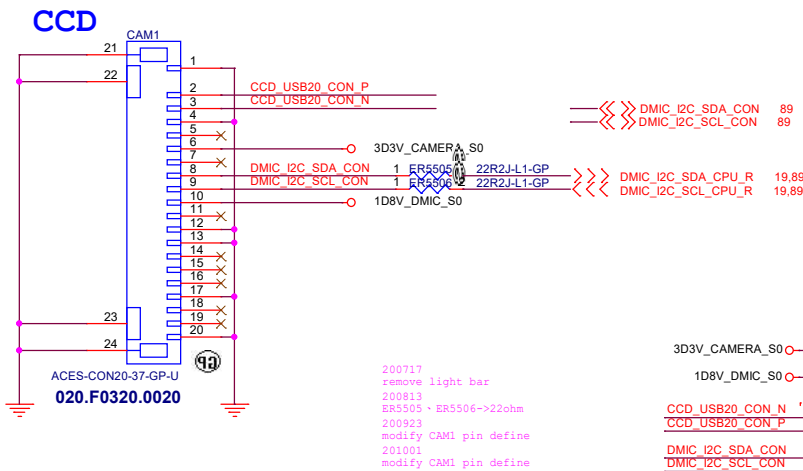
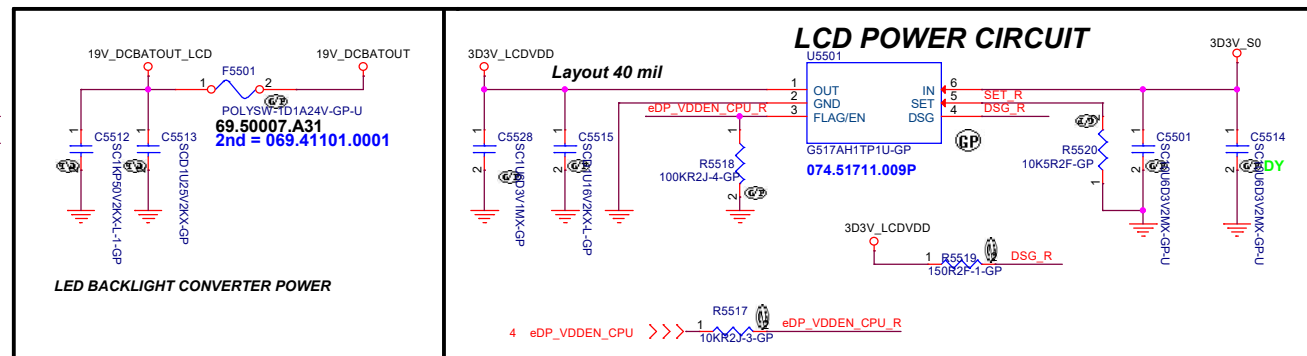
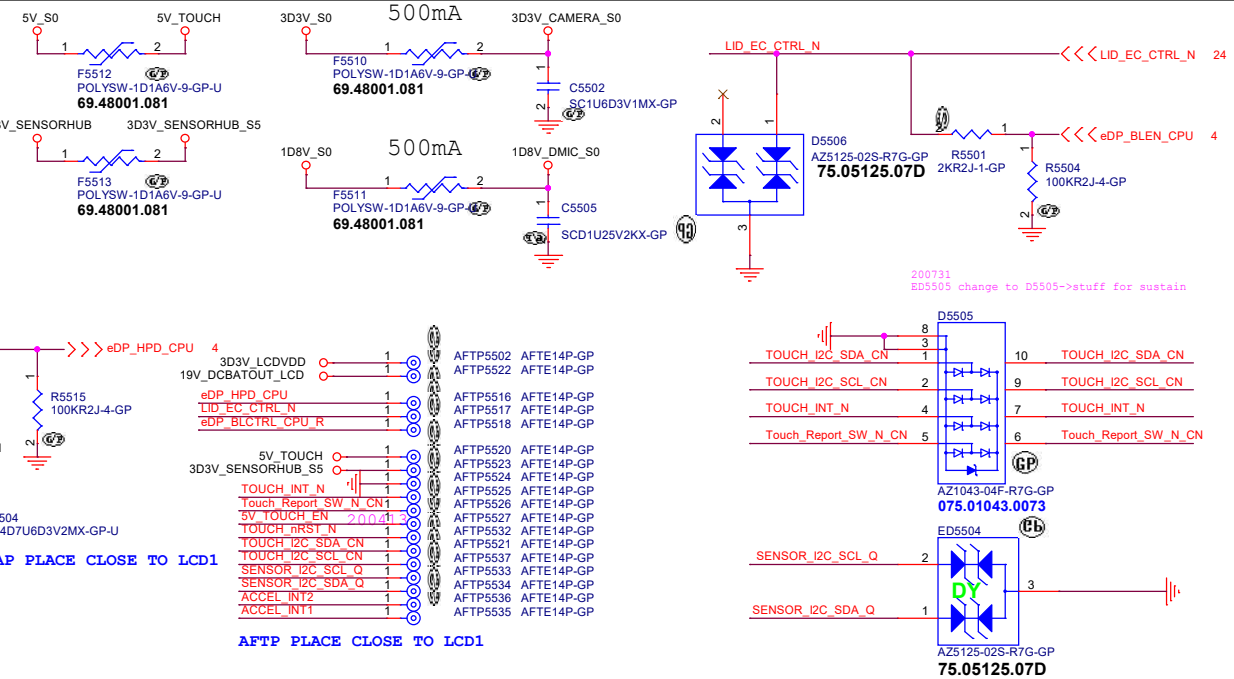
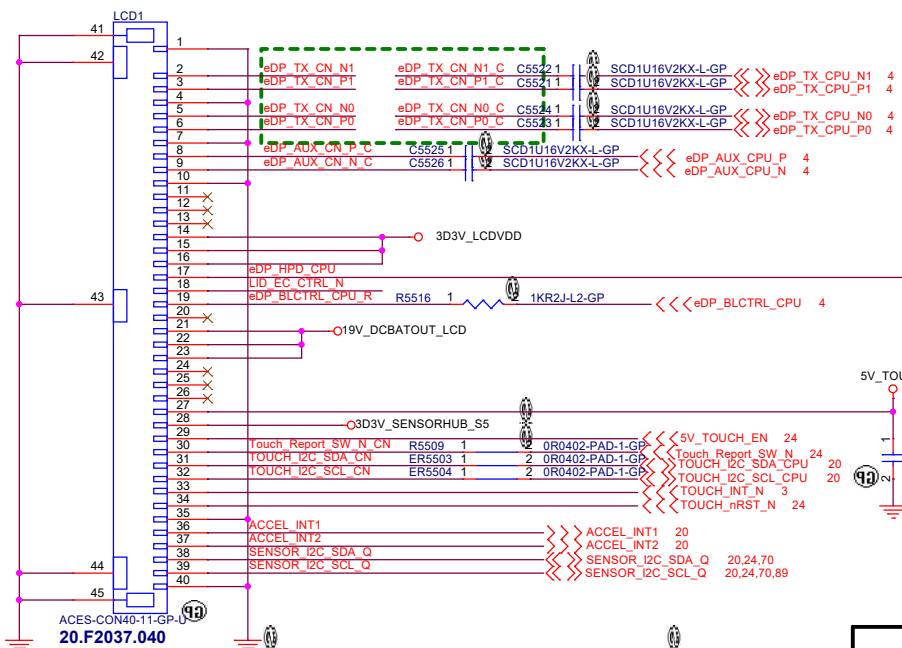
## Slinky TGL 14" Pavlion

Date: Friday, December 04, 2020

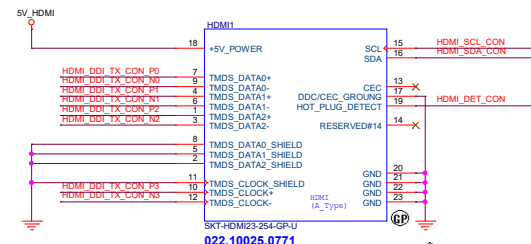
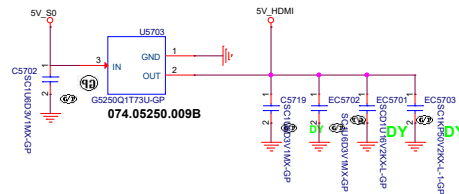
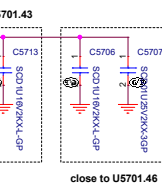
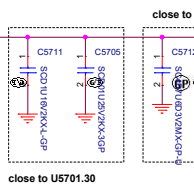
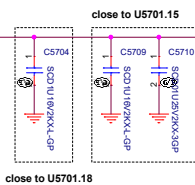
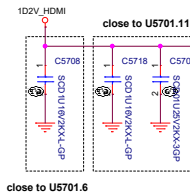
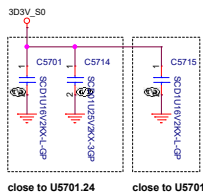
Sheet 53 of 106



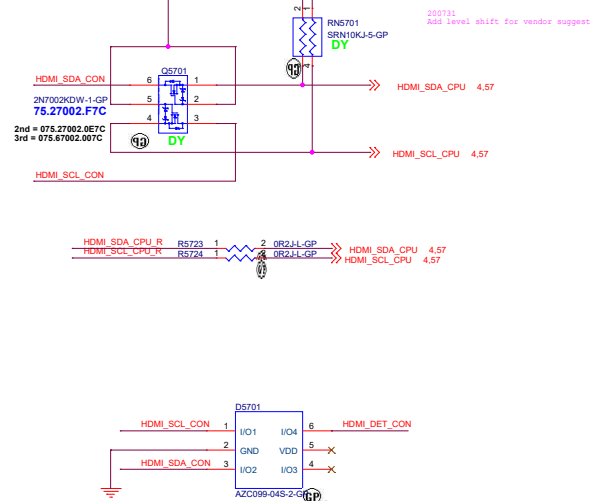
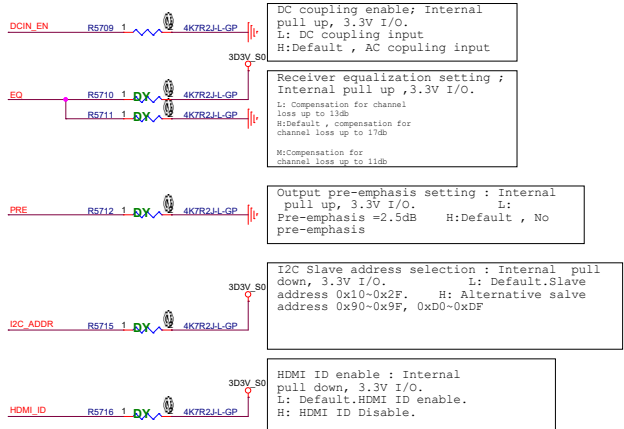
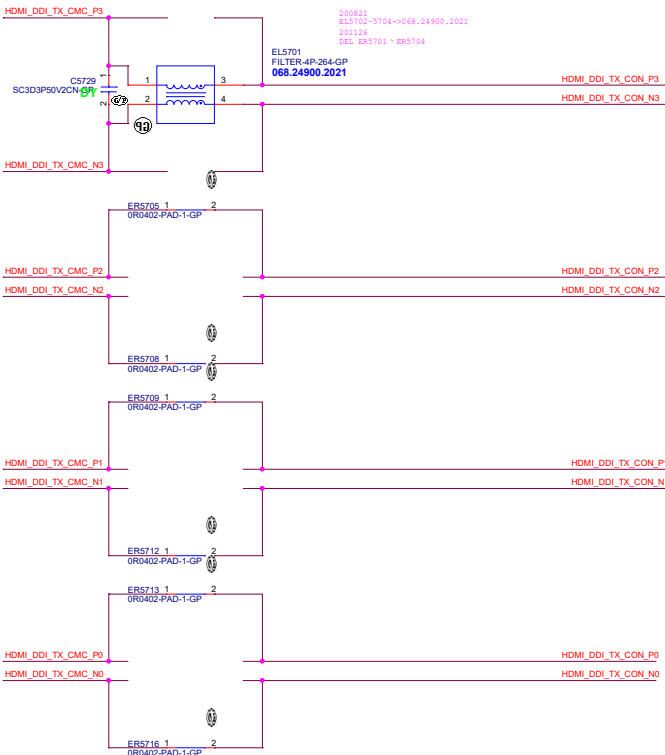
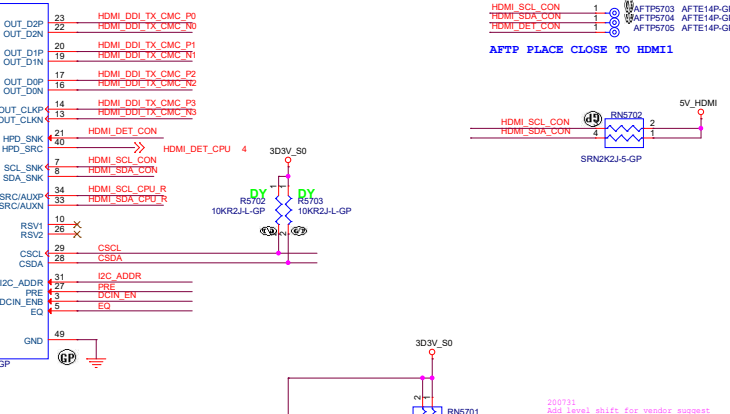
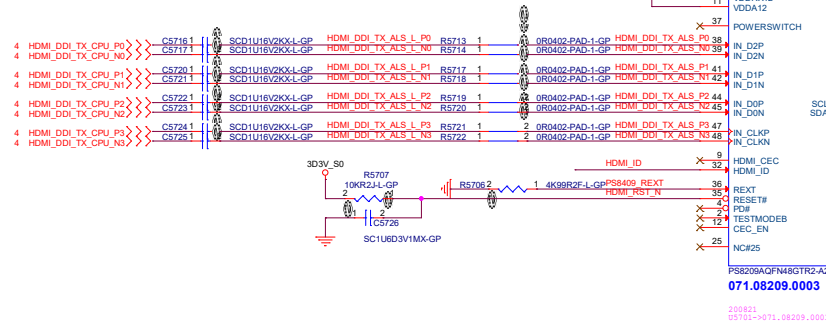
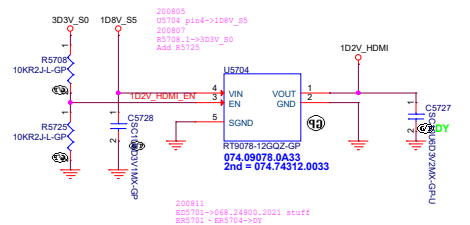
## eDP + G-sensor + Touch Connector



# HDMI Conn



## For HDMI 1D2V

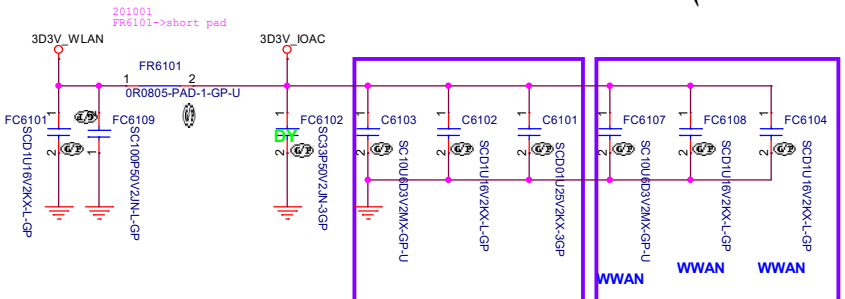


(Blanking)

<Core Design>

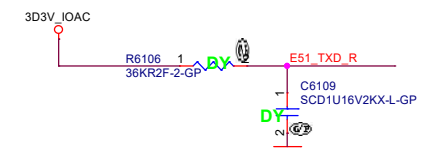
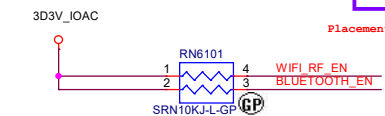
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
INT IO (HDD/ODD)		
Size	Document Number	Rev
A4	Slinky TGL 14" Pavlion	-1
Date:	Friday, December 04, 2020	Sheet 60 of 106

### *Mini Card Connector(802.11a/b/g/n)*



Placement close to WLAN1 Pin2 and 4      Placement close to WLAN1 Pin70 and 72

Layout sequence is 10uF => 0.1uF => 0.01uF

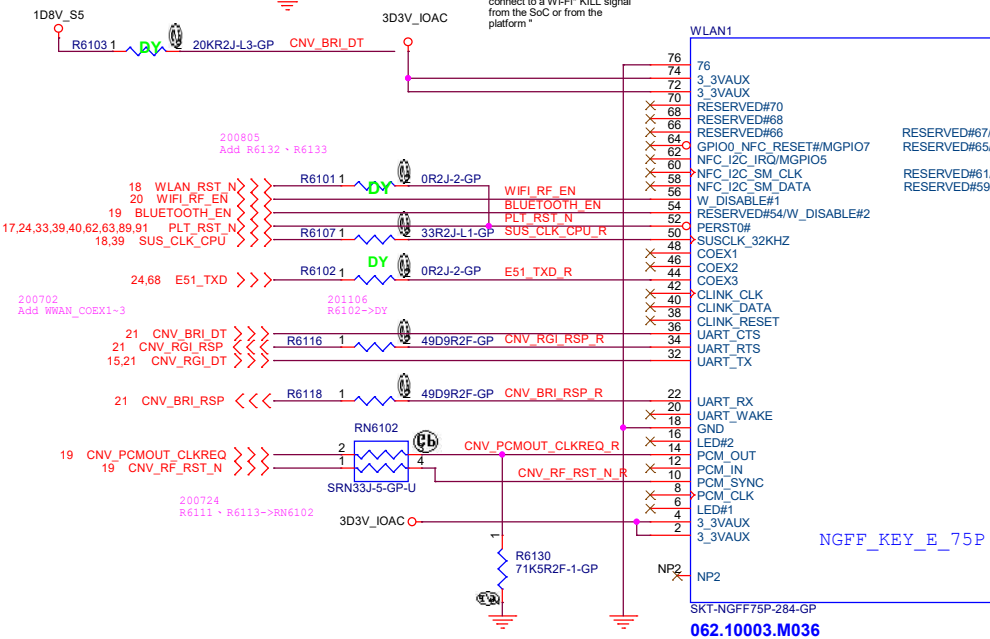


**BLUETOOTH\_EN(Pin 54)**

"BT\_KILL input. Optional to connect to a Bluetooth KILL signal from the SoC or from the platform"

WIFI\_RF\_EN(Pin 56)

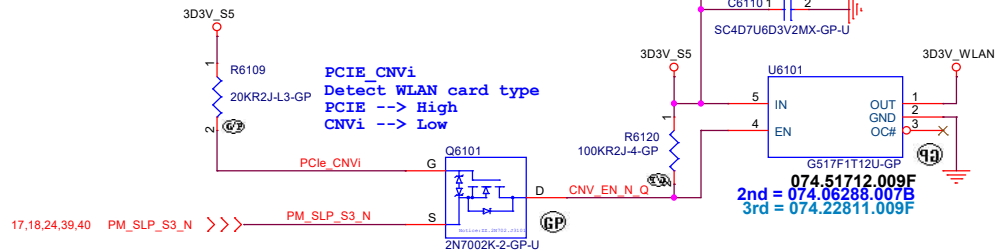
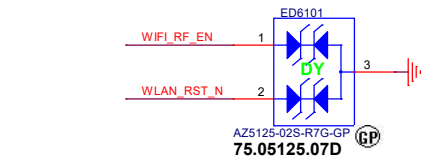
"WLAN\_KILL" Input: Optional to connect to a Wi-Fi\* KILL signal from the SoC or from the platform "



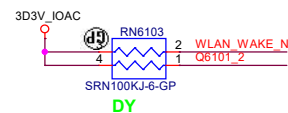
NGFF KEY E 75P

062.10003.M036

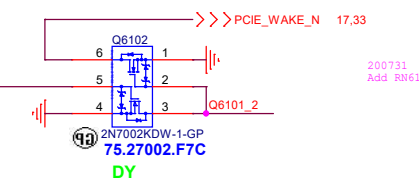
```
200724
WLAN1->062.10003.M036 for CE
```



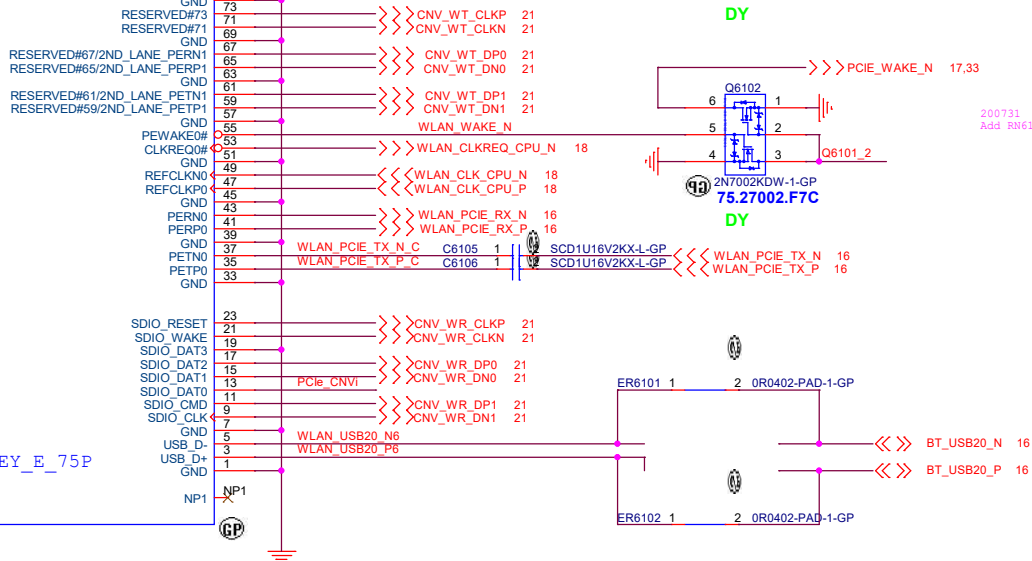
2nd = 074.06288.007B  
3rd = 074.22811.009F



200731  
Add RN6103 and Q6102 for CM01



75.27002.F7C  
DY



PLT\_RST\_N 1 AFTP6101 AFTE14P-GP

### <Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

[illegible]

## **INT IO (WLAN M.2)**

Size

Document Number

### **Slinky TGL 14" Pavlion**

Date: Friday, December 04, 2020

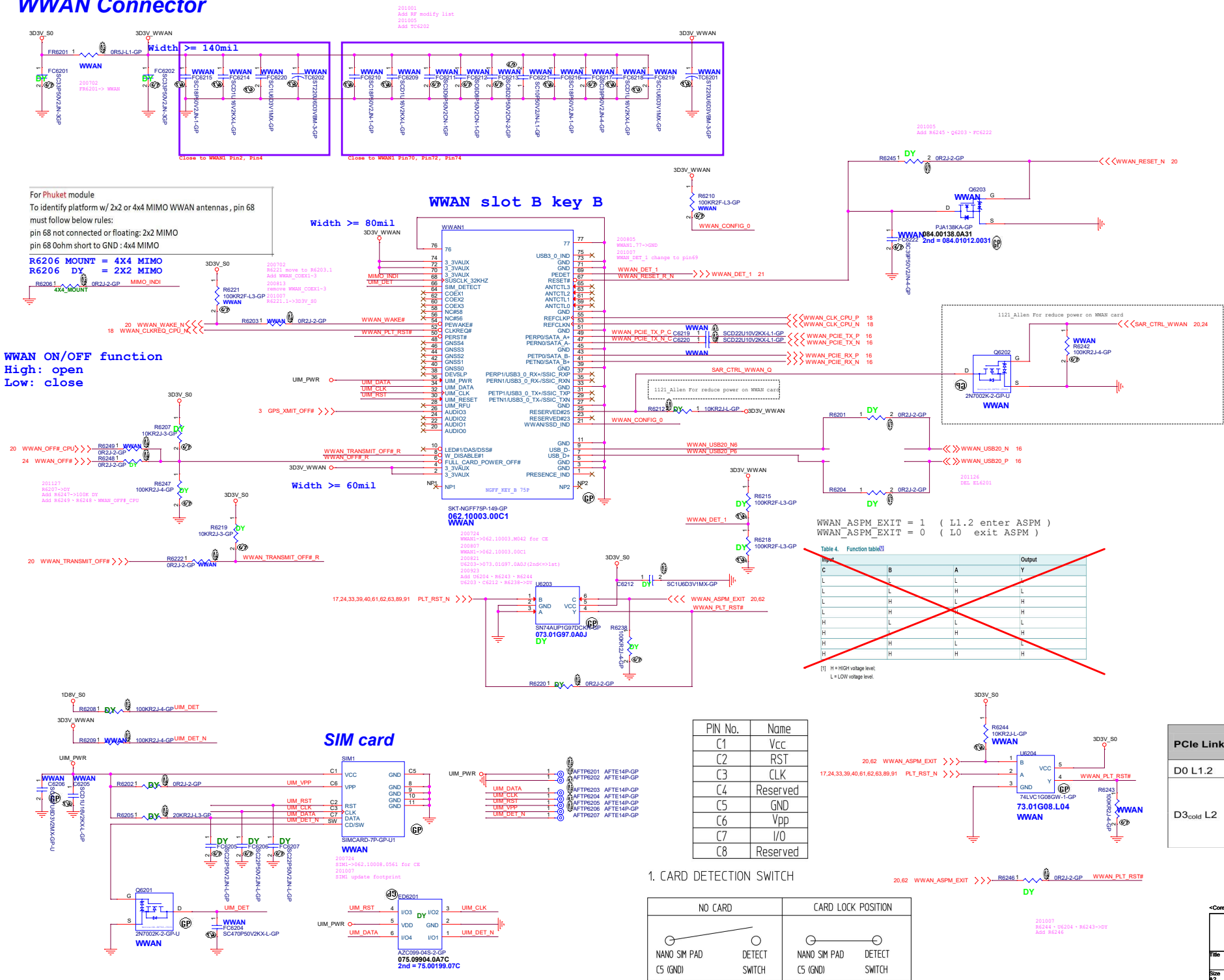
Sheet

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Rev	
-----	--

106



## WWAN Connector



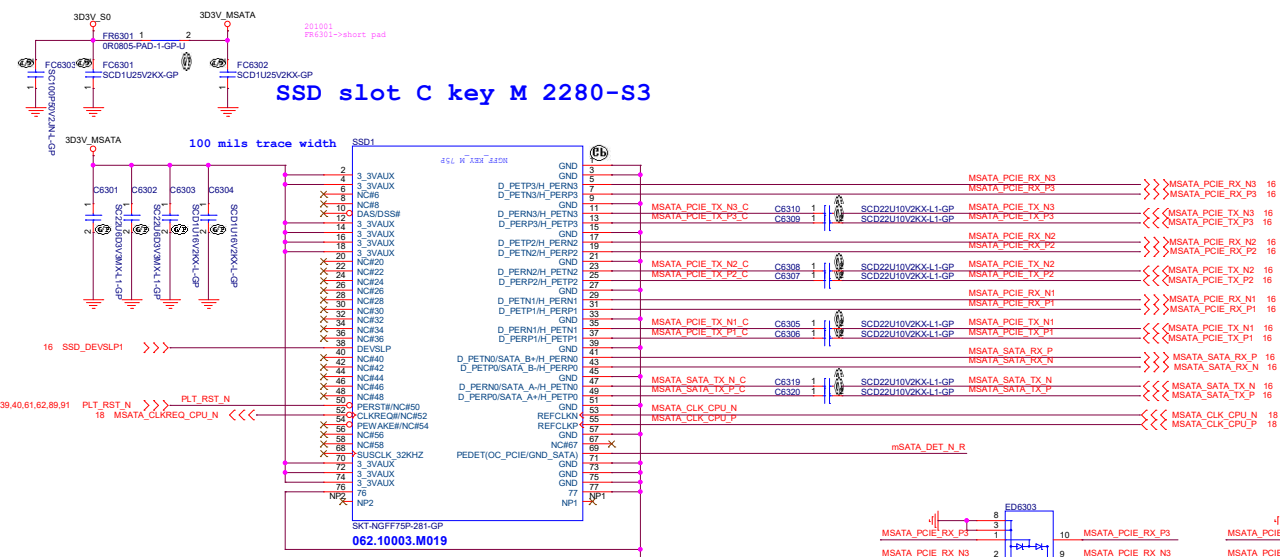
PCIe Link State	PERST#	CLKREQ#
D0 L1.2	H	H
D3 <sub>cold</sub> L2	L	H
	L	L

PIN No.	Name
C1	Vcc
C2	RST
C3	CLK
C4	Reserved
C5	GND
C6	Vpp
C7	I/O
C8	Reserved

### 1. CARD DETECTION SWITCH

NO CARD		CARD LOCK POSITION	
			
NANO SIM PAD C5 (GND)	DETECT SWITCH	NANO SIM PAD C5 (GND)	DETECT SWITCH

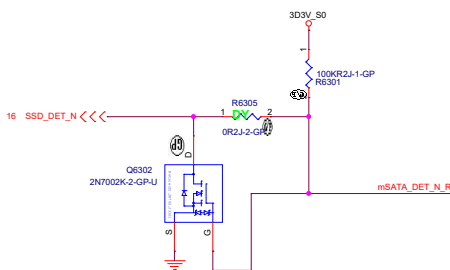
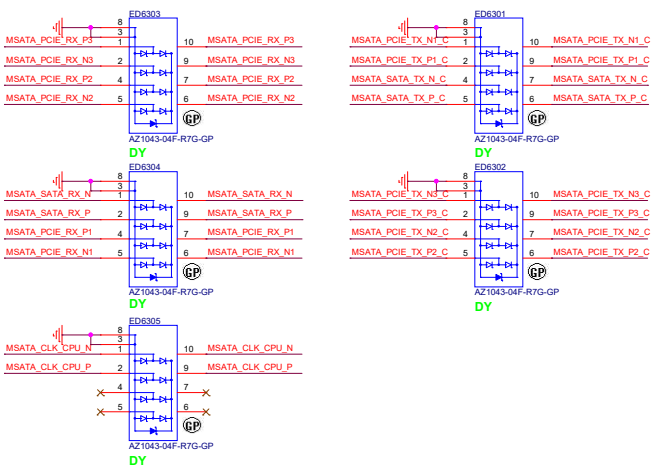
NGFF Connector



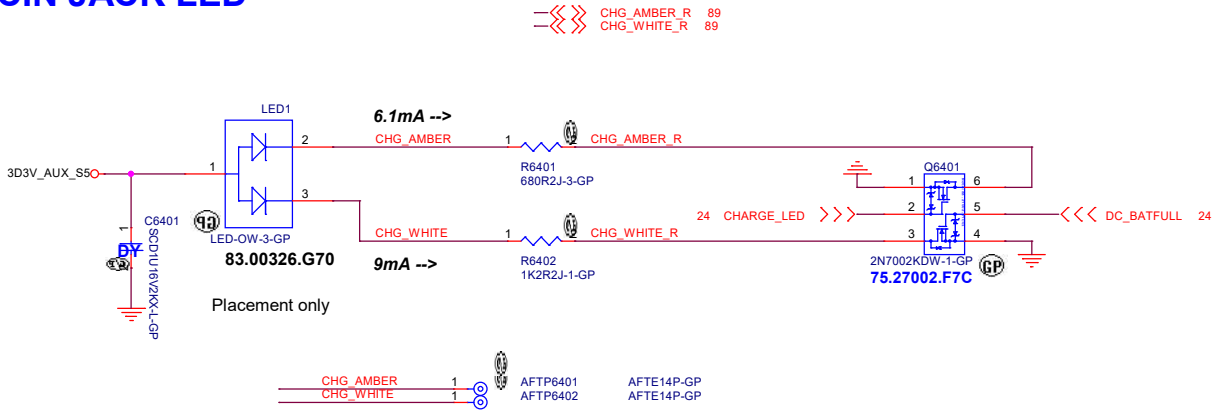
mSATA_DET_N_R		
0		SATA
X		PCIe

20150713 Add Truth Table and modify direction

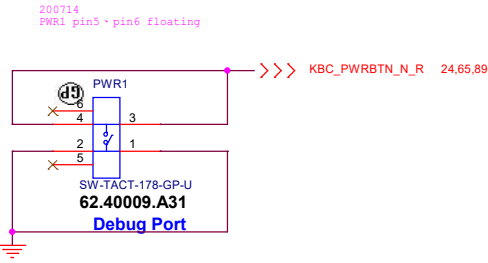
8	N/C	N/C
10	LED1#	Device Active Signal
12	3.3V	3.3V source



DCIN JACK LED



Power Button



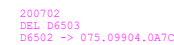
Light Bar

200717  
remove light bar

## Key Board conn.



075.09904.0A7C

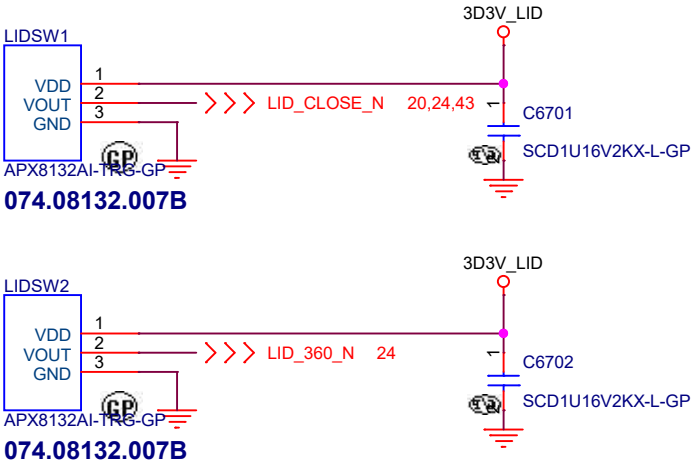


AFTP PLACE CLOSE TO KBL1

Title			
<b>INT IO (KB/TP)</b>			
Size A3	Document Number		Rev
	<b>Slinky TGL 14" Pavlion</b>		<b>-1</b>
Date:	Friday, December 04, 2020	Sheet 65 of	106



# HALL SENSOR



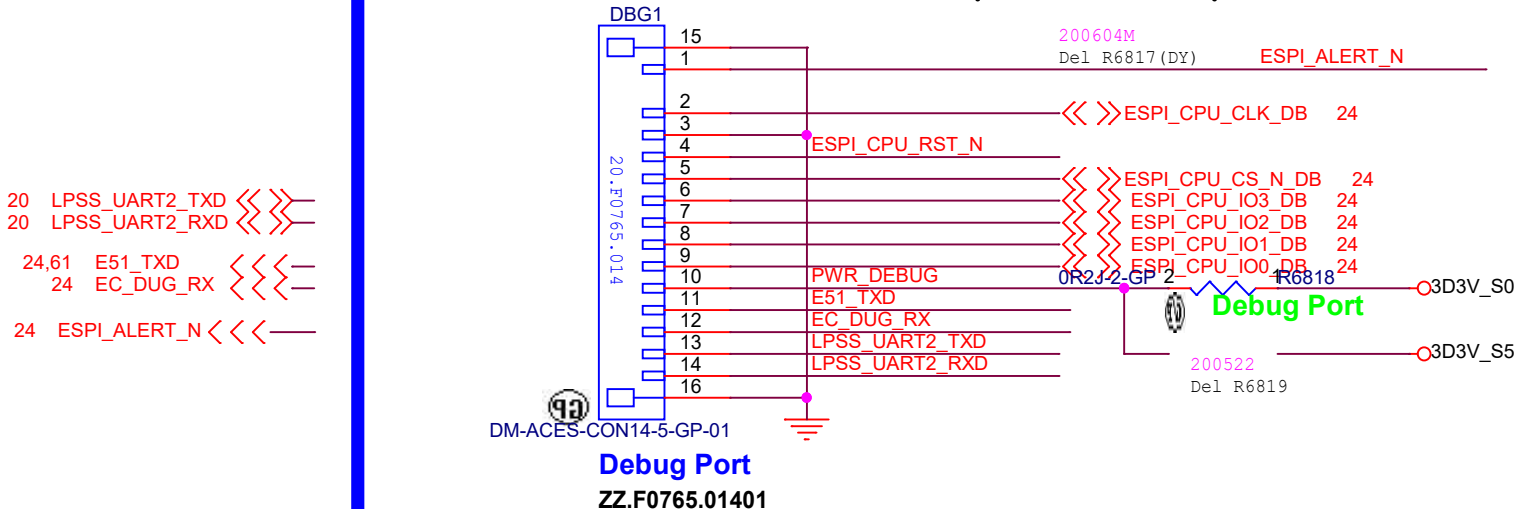
<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Sensor (RSVD) (Hall-Sensor)</div>		
Size <div>A4</div>	Document Number <div>Slinky TGL 14" Pavilion</div>	Rev <div>-1</div>
Date: Friday, December 04, 2020		
Sheet 67 of 106		

Refer bandon ICL Page68

18,24,39 ESPI\_CPU\_RST\_N >>>—

ESPI DEBUG (Wistron)



201123  
DBG1->ZZ.F0765.01401

<Core Design>

Title		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Size		Document Number	
A		Slinky TGL 14" Pavlion	
Date:		Friday, December 04, 2020	
		Sheet 68 of 106	
		Rev -1	

G-SENSOR

To KBC  
for Cool sense

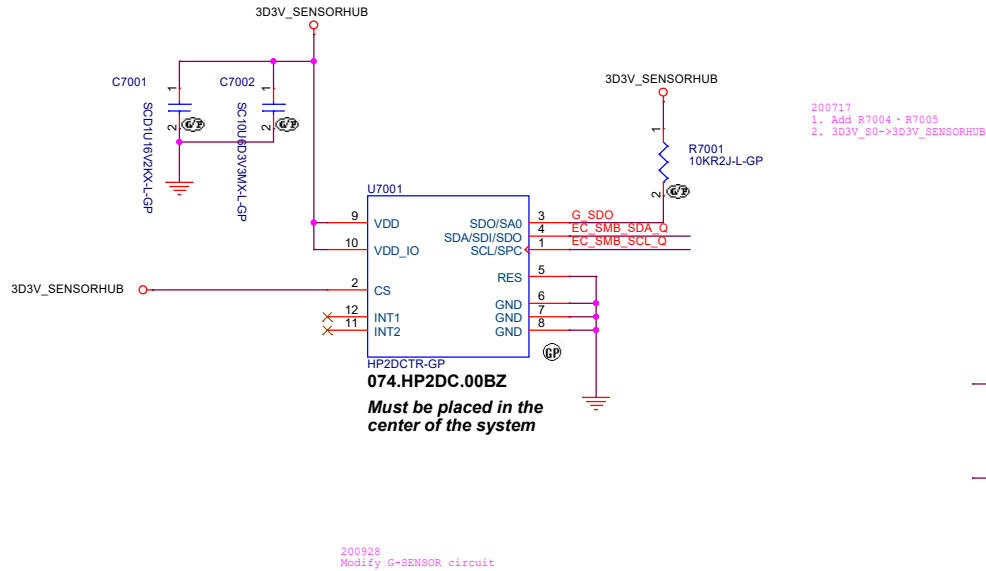
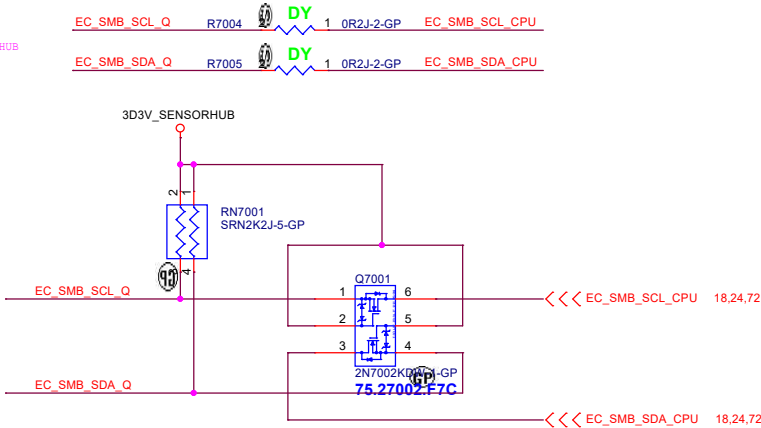


Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)



To Sensor HUB  
for LCD angle

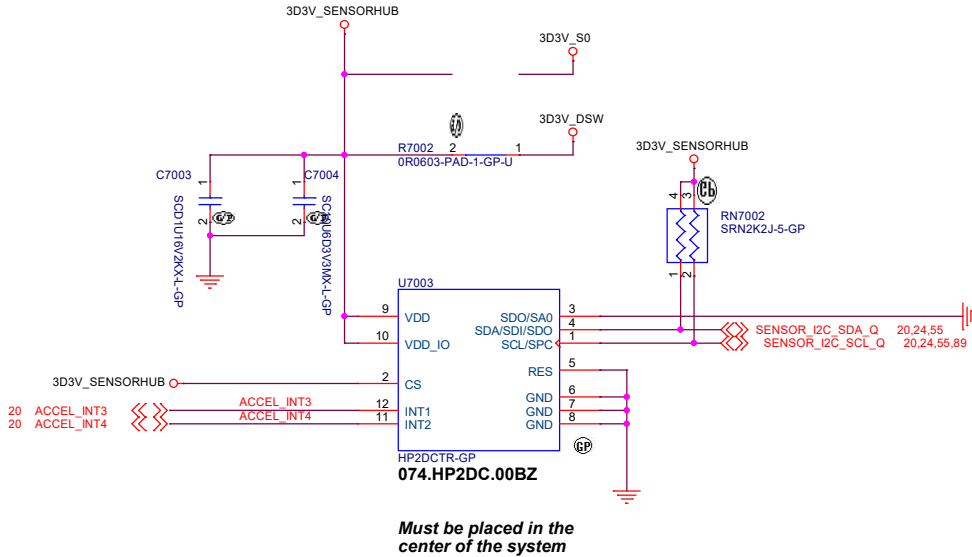
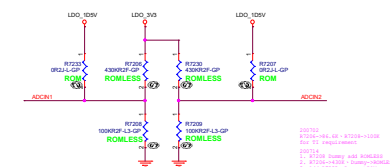
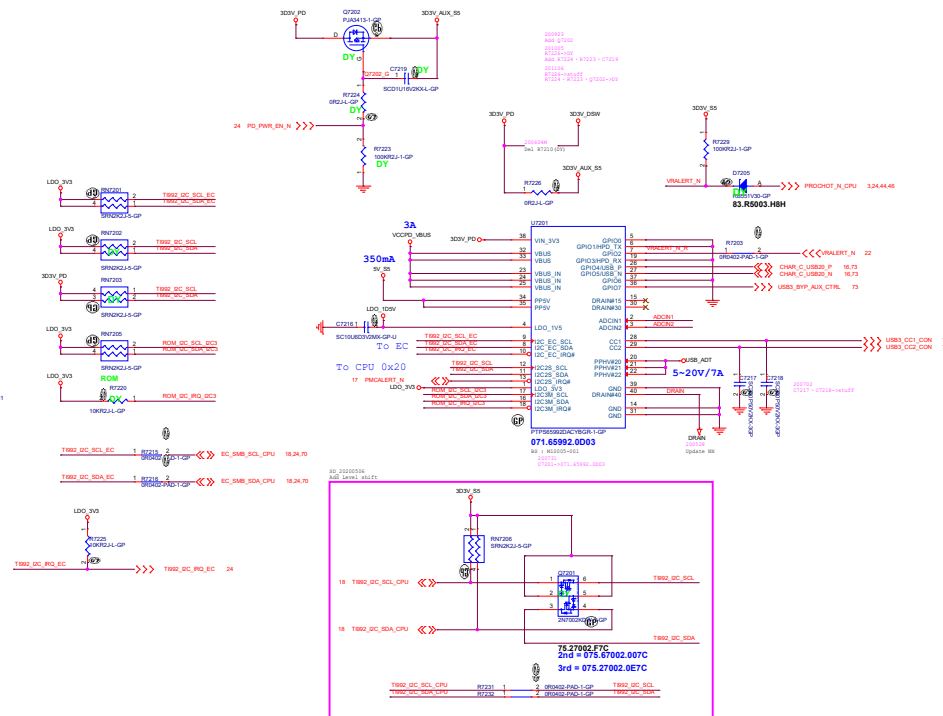
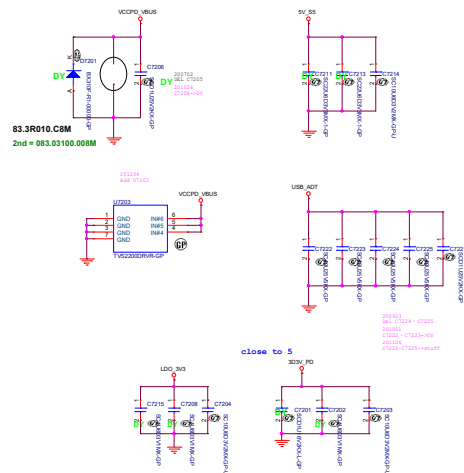


Table 13. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

<Core Design>



## Device Functional Modes (continued)

Table 6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value <sup>(1)</sup>	ADCIN2 decoded value <sup>(1)</sup>	IPC address Index <sup>(2)</sup>	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	
4	4	#2	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
3	0	#3	
2	7	#4	
7	6	#1	
6	6	#2	
6	5	#3	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	7	#4	
7	3	#1	
3	3	#2	
0	0	#3	
3	7	#4	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V.
7	0	#1	
7	0	#2	
6	0	#3	
5	7	#4	
			SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode.

Table 2. Decoding of ADCIN1 and ADCIN2 Pins

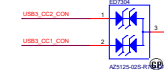
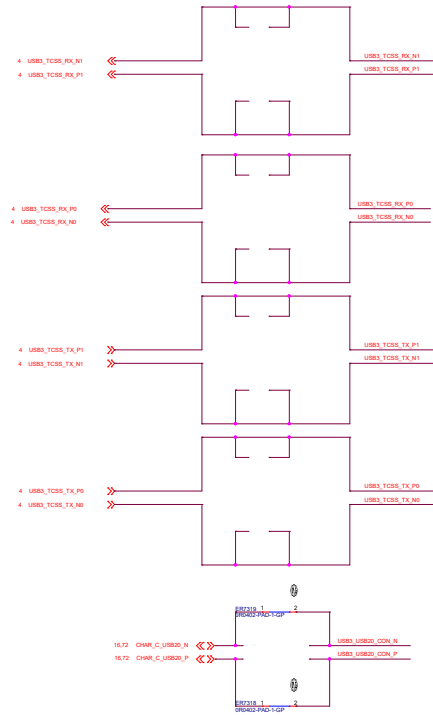
DIV = R <sub>DOWN</sub> / (R <sub>UP</sub> + R <sub>DOWN</sub> ) <sup>(1)</sup>			Without using R <sub>UP</sub> or R <sub>DOWN</sub>	ADCI <sub>Nx</sub> decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.9062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

Table 5. I<sup>2</sup>C Default Slave Address for I2C EC\_SCL/SDA

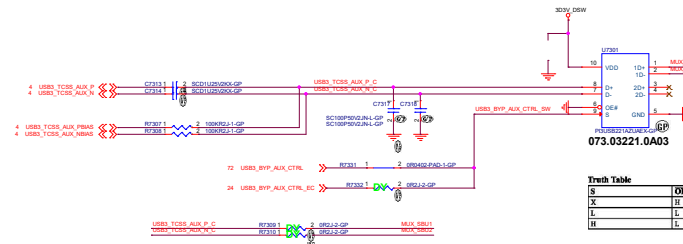
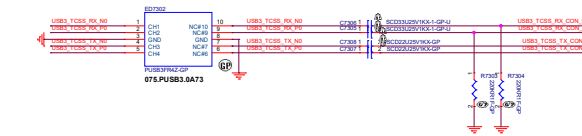
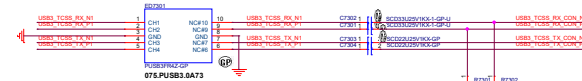
I <sup>2</sup> C address index (decoded from ADC1N1 and ADC1N2) <sup>(1)</sup>	Slave Address								Available During BOOT
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1	0	1	0	0	0	0	0	R/W	Yes
#2	0	1	0	0	0	0	1	R/W	Yes
#3	0	1	0	0	0	1	0	R/W	Yes
#4	0	1	0	0	0	1	1	R/W	Yes

(1) See Table 2 details about ADCIN1 and ADCIN2 decoding

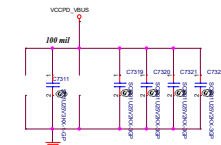
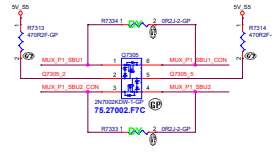
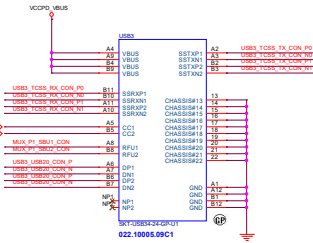
# USB Type C Connector OUTPUT=3A



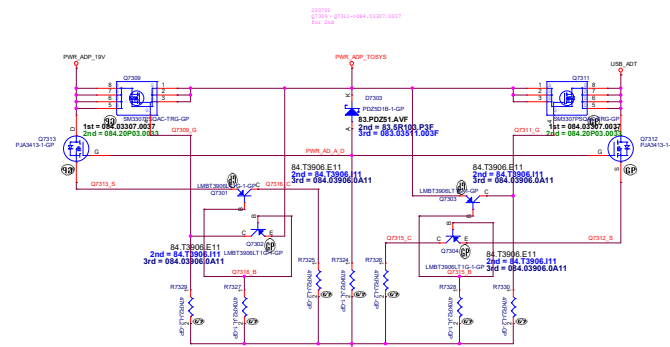
075.09904.0A7C



S	OE	Function
1	0	Disconnect
2	1	D = 1D
3	1	D = 2D



ATF PLACE CLOSE TO USB3



075.09904.0A7C

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Main Func = dGPU

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GPU_PEG (1/5)			
Size	Document Number	Rev	
A2	Slinky TGL 14" Pavilion	-1	
Date: Friday, December 04, 2020 Sheet 76 of 108			

Main Func = dGPU

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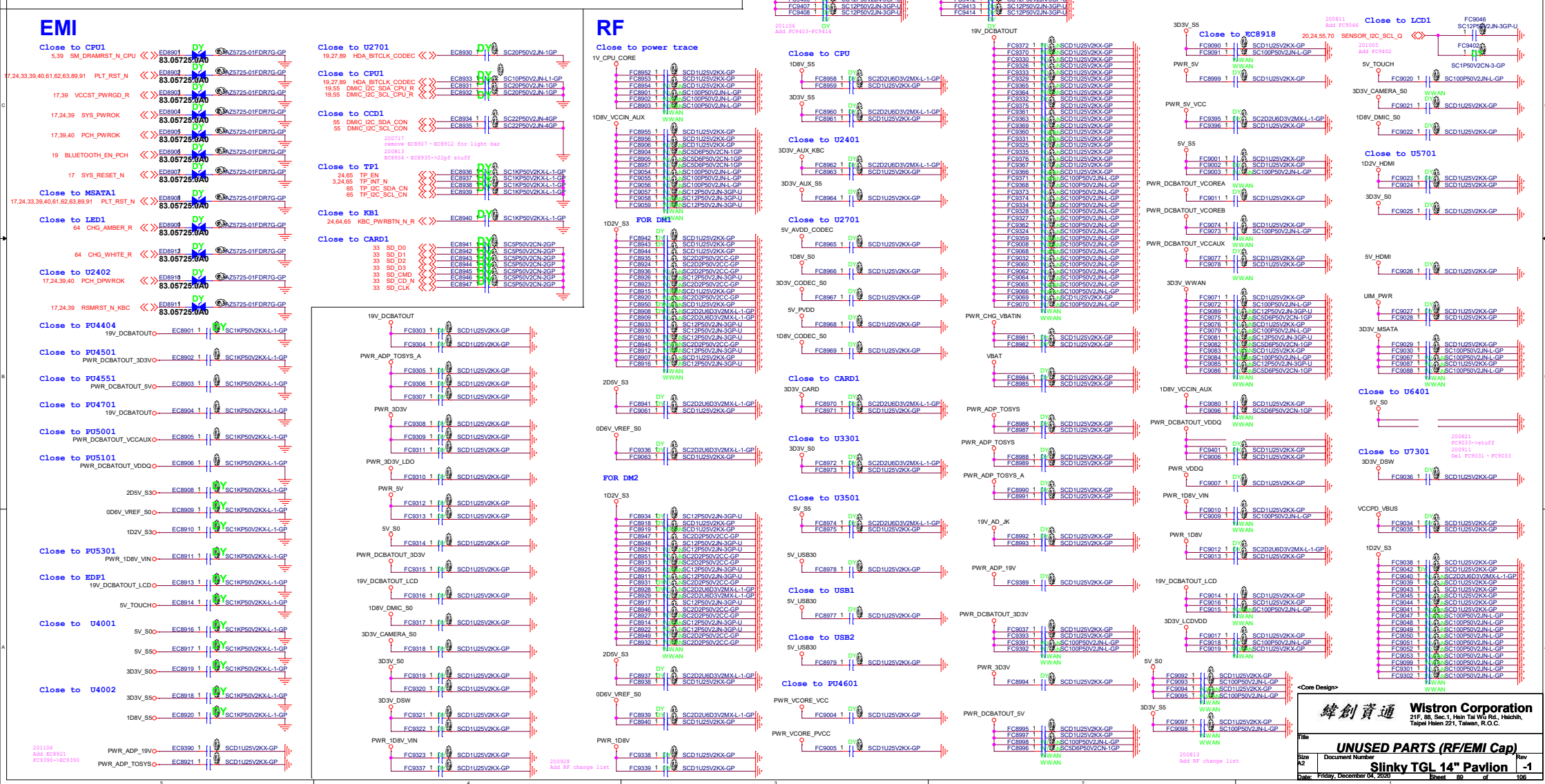
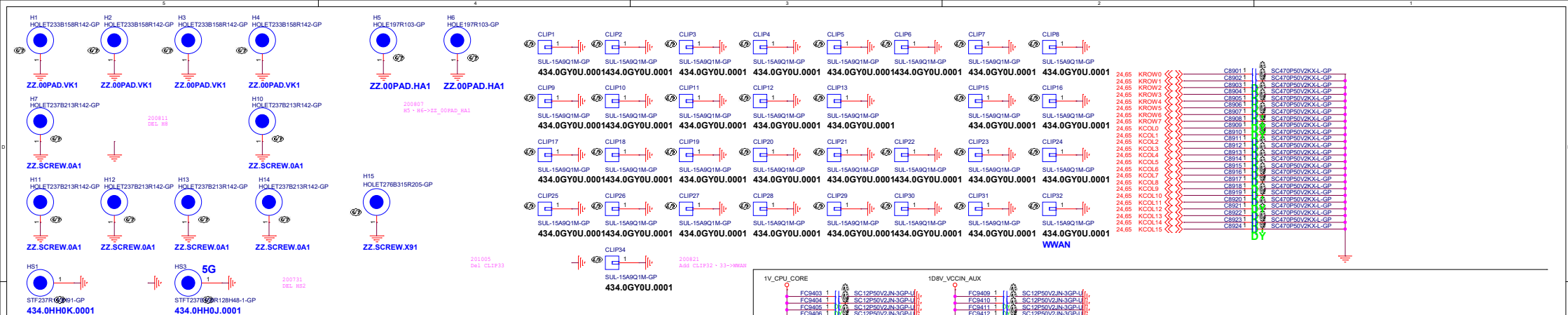
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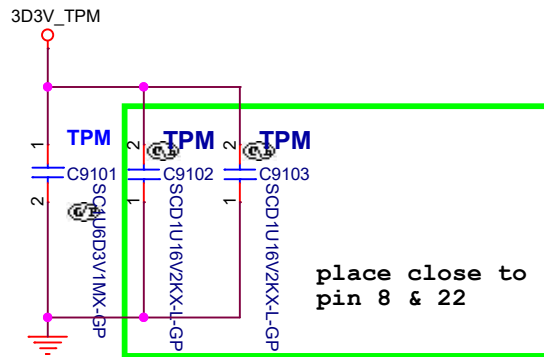




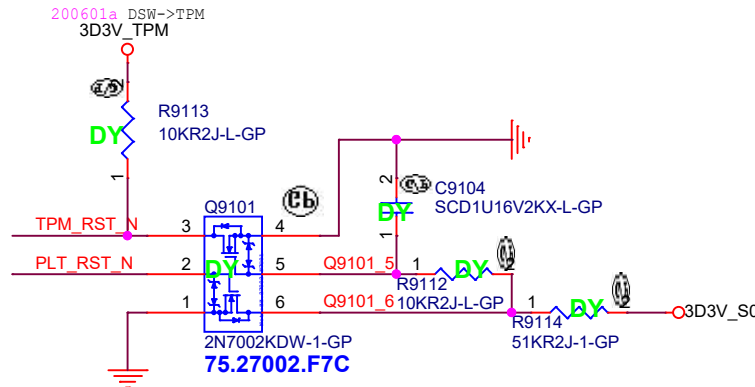
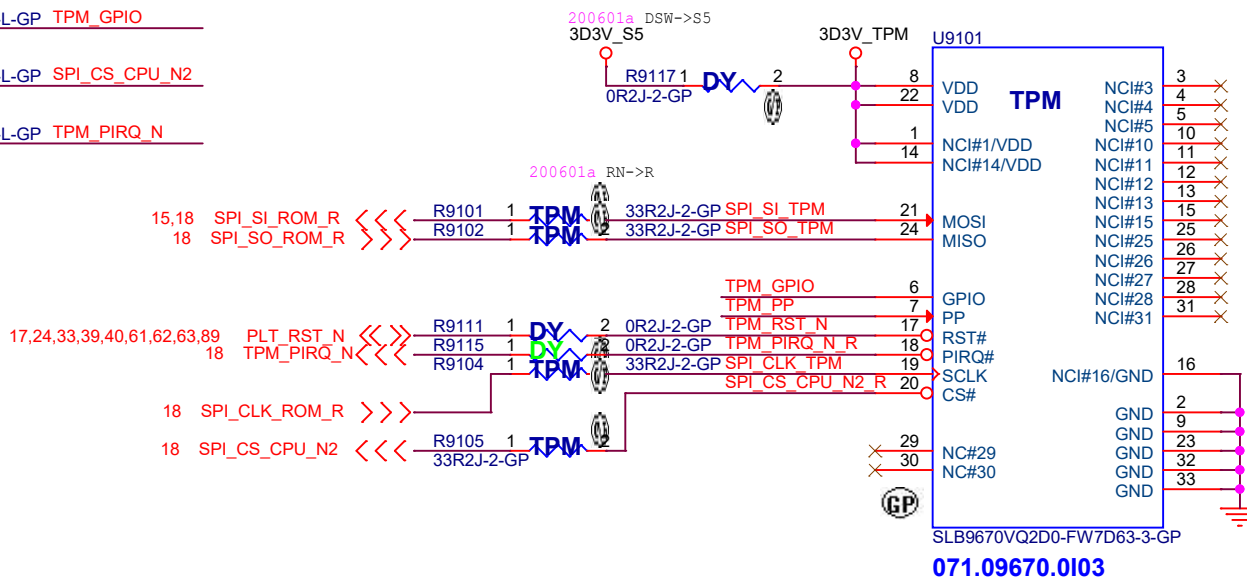
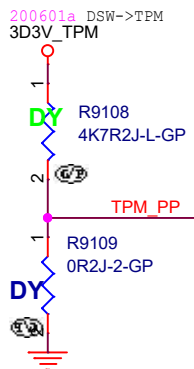


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24 SPI\_CLK\_TPM >>> SPI\_CLK\_TPM  
 24 SPI\_SI\_TPM >>> SPI\_SI\_TPM  
 24 SPI\_SO\_TPM <<< SPI\_SO\_TPM



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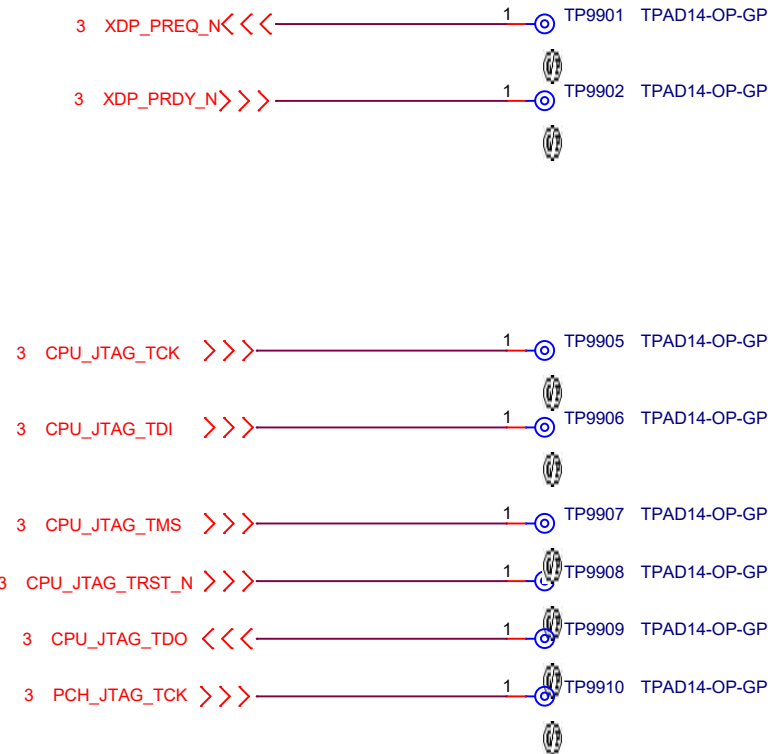
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Size		Document Number			<b>Slinky TGL 14" Pavilion</b>					Rev <b>-1</b>	
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Front Facing Camera Module Conn.

(Blanking)

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Follow NTD Net name



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**Debug (HDT debug)**

Size  
A4

Document Number

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**-1**

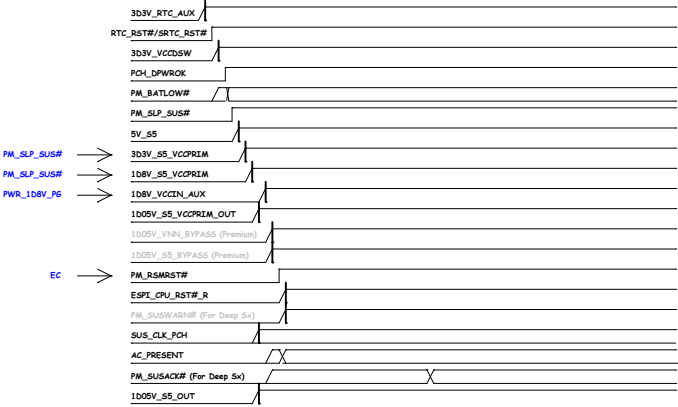
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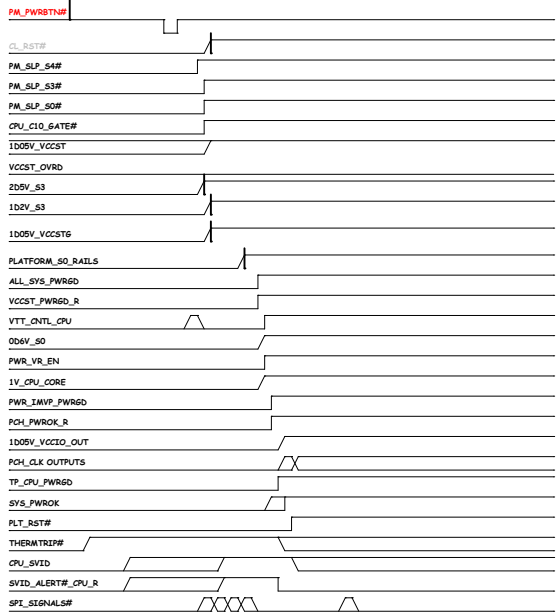
Intel-Power Up Sequence

#507872 Rev1.0 P.417

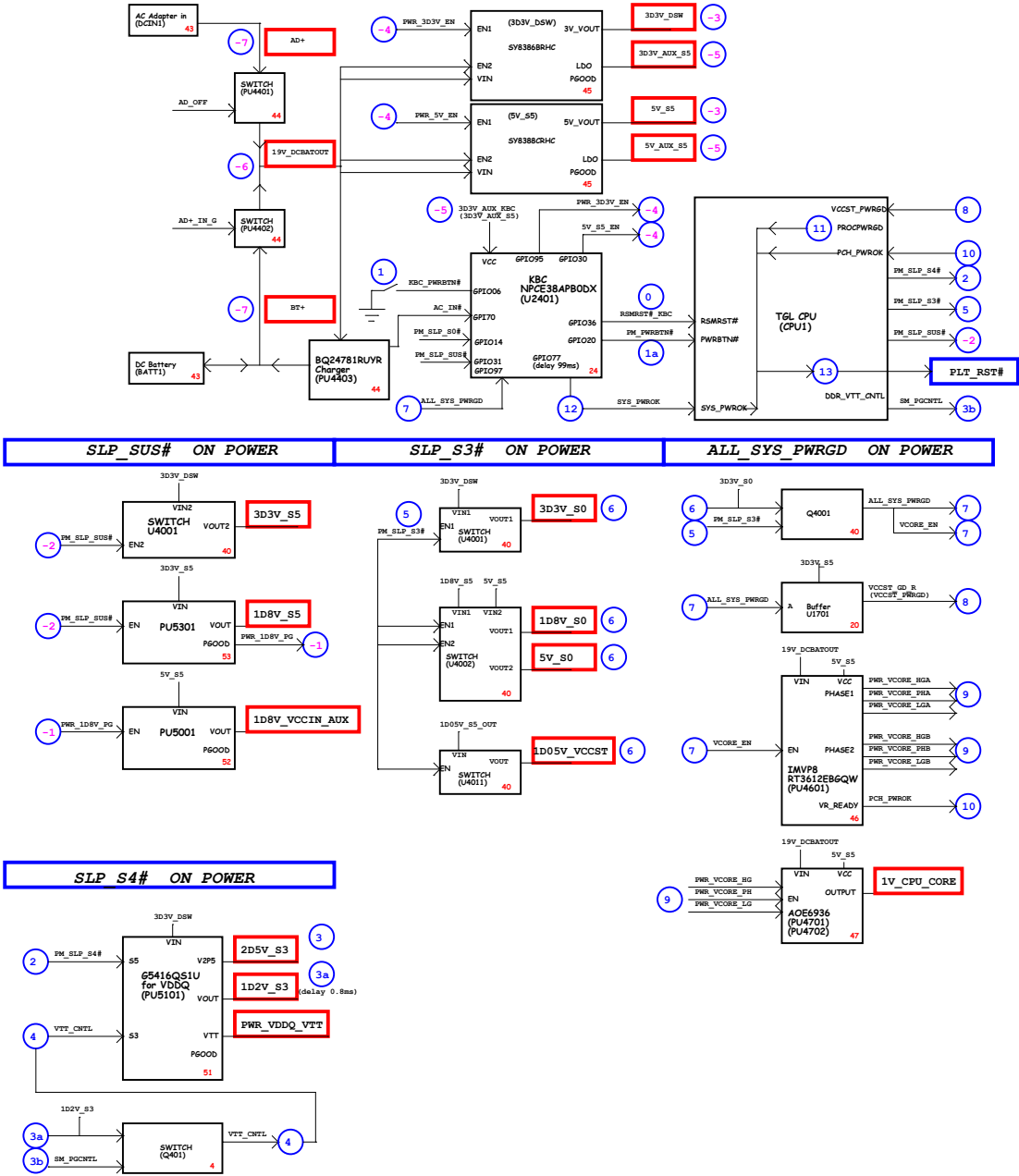
G3 to S5 Sequence Flow



S5 to S0 Sequence Flow

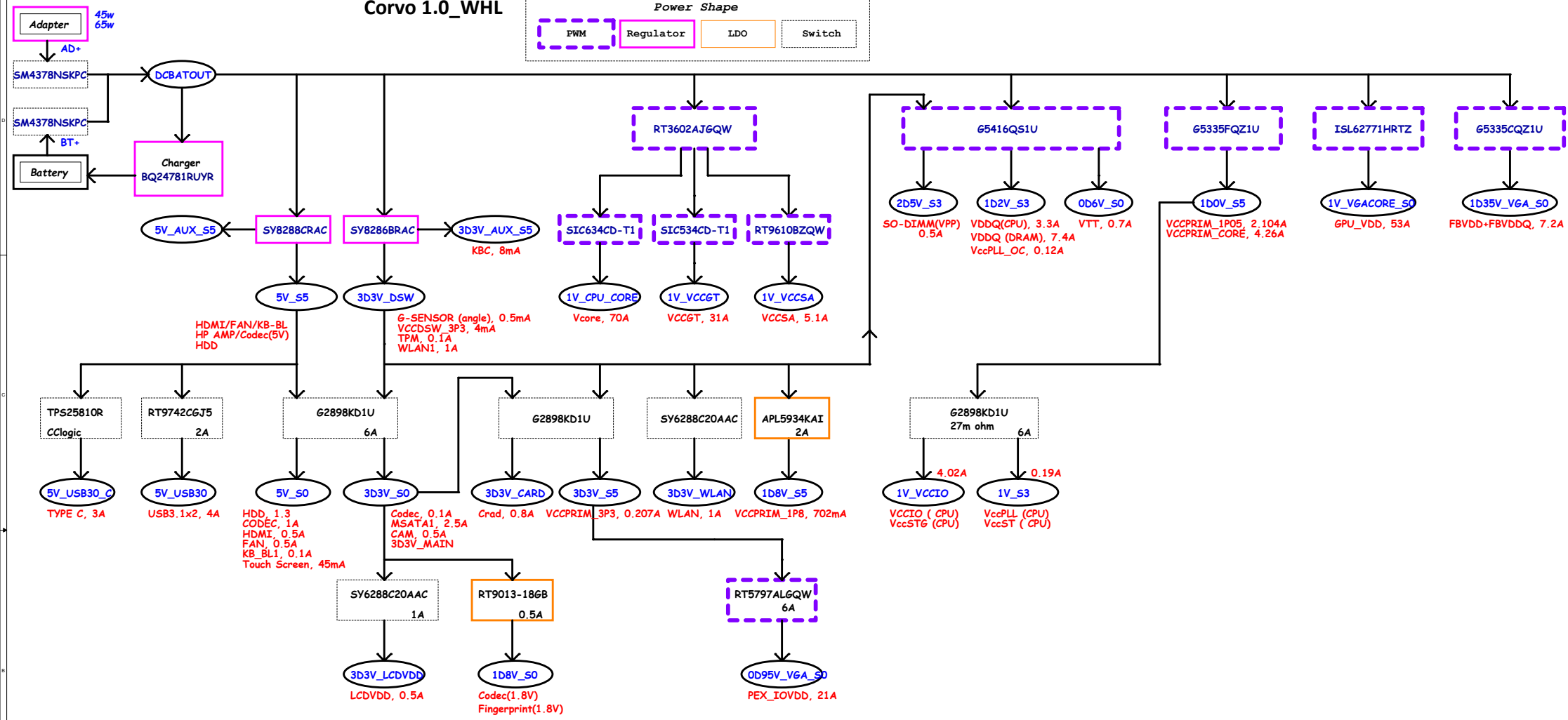
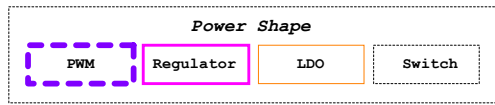


TGL U POWER UP SEQUENCE DIAGRAM

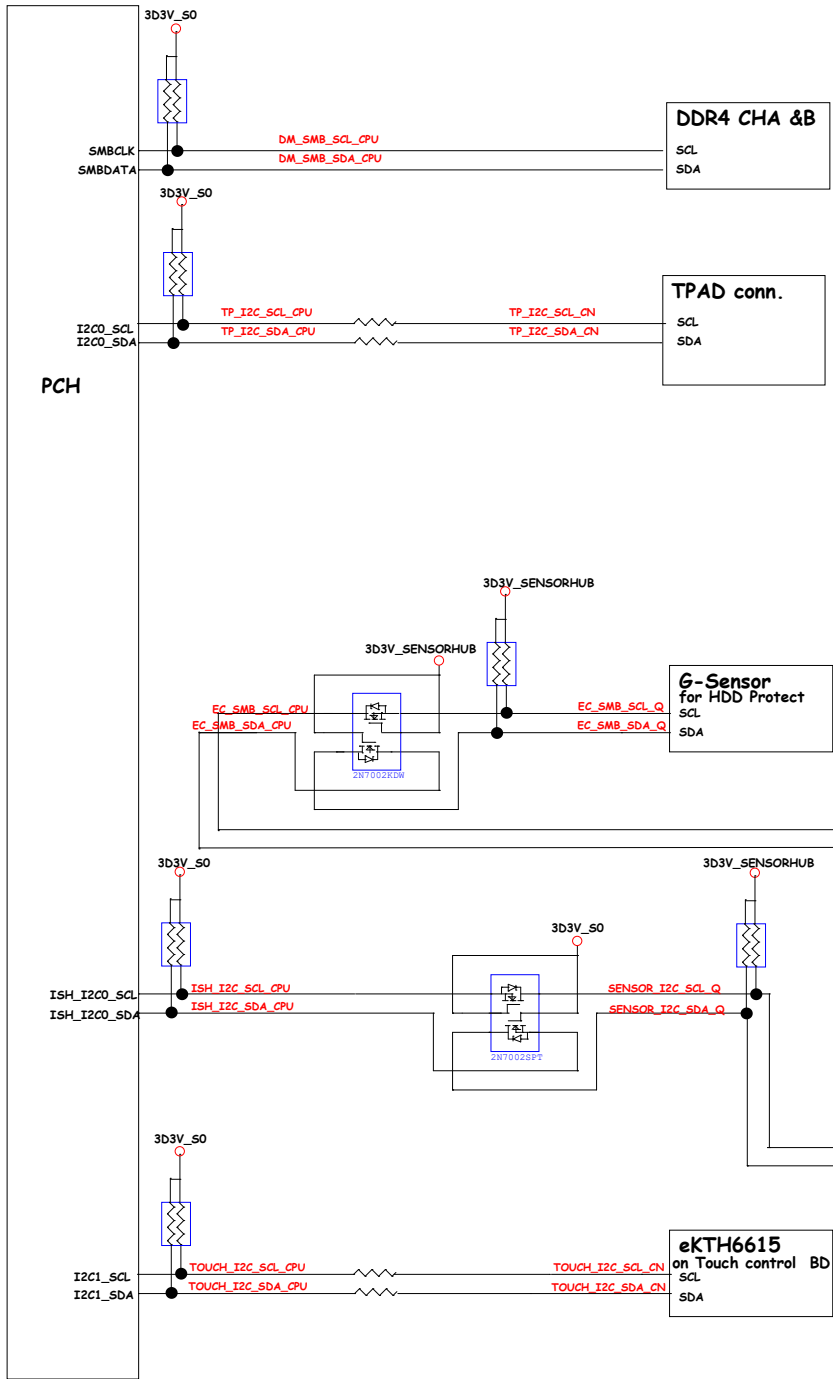




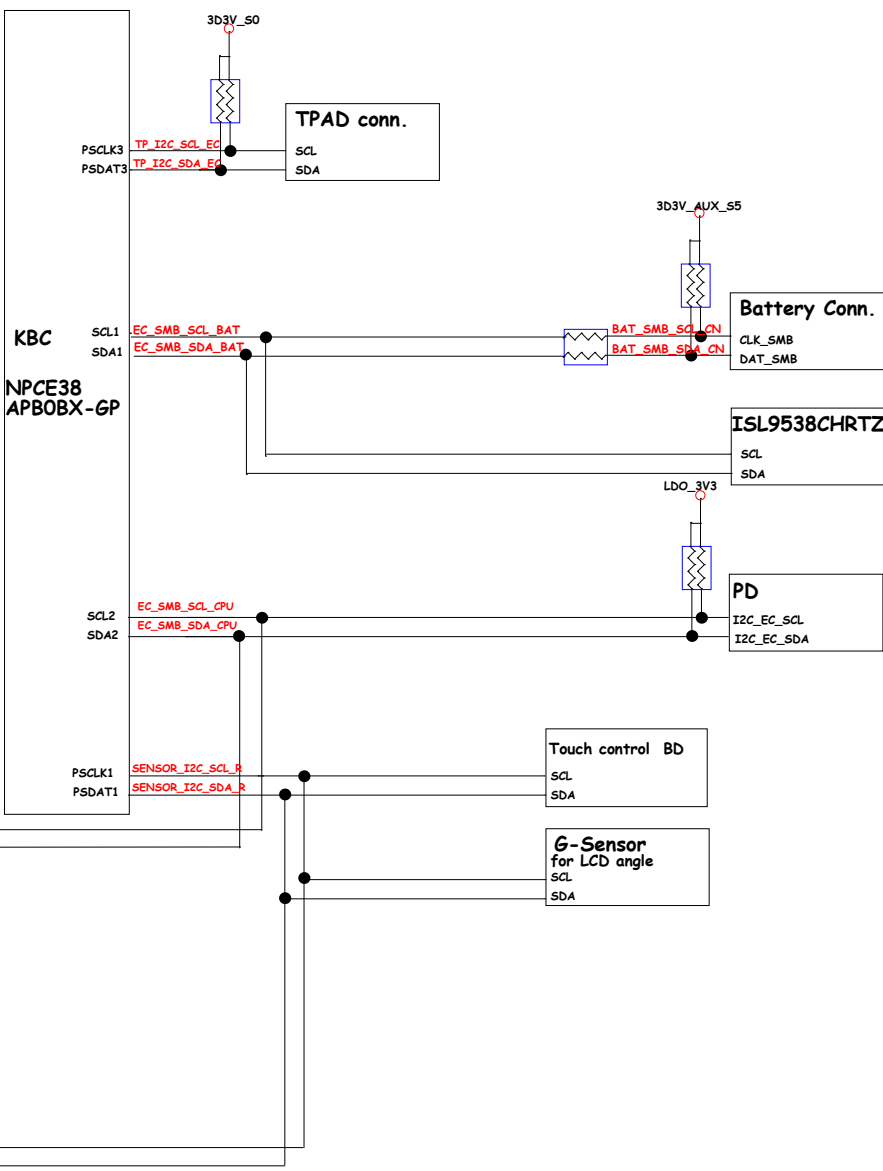
# Corvo 1.0\_WHL



PCH SMBus/ I2C Block Diagram



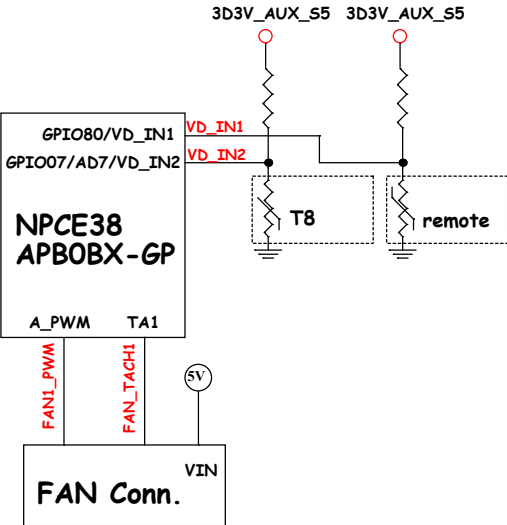
KBC SMBus/ I2C Block Diagram



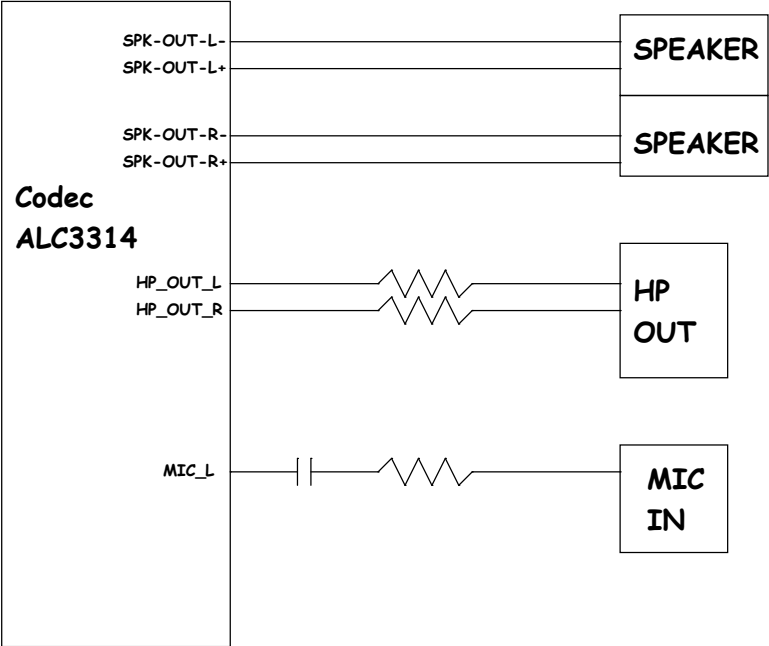
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# Thermal Block Diagram



# Audio Block Diagram



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<b>Title</b> <b>THERMAL/AUDIO BLOCK DIAGRAM</b>			
<b>Size</b> A3	<b>Document Number</b> <b>Slinky TGL 14" Pavilion</b>		<b>Rev</b> <b>-1</b>
<b>Date:</b> Friday, December 04, 2020	<b>Sheet</b> 105	<b>of</b> 106	